

Document Title**4Mx16 bit Synchronous Burst Uni-Transistor Random Access Memory**Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial Draft - Design target	March 11, 2004	Advance
0.1	Revised - Deleted Deep Power Down Mode support	April 19, 2004	Advance
0.2	Revised - Changed product code from K1B6416B7C into K1B6416B6C	May 10, 2004	Advance
0.3	Revised - Filled out Package type(54ball FBGA 6.0mm x 8.0mm) - Changed Hi-Z parameters(tCHZ, tOHZ, tBHZ, tWZ) from Max.7ns into Max.12ns and changed tHZ from Max.10ns into Max.12ns - Updated "Fig.17 TIMING WAVEFORM OF WRITE CYCLE(1)" in page 23 - Added comment on standby current(IsB1) measure condition as "Standby mode is supposed to be set up after at least one active operation after power up. IsB1 is measured after 60ms from the time when standby mode is set up." - Added comment on restriction of the transition between Asynchronous Write operation and Fully Synchronous bus operation(Page 10,11) - Filled out IsB1 value, IsBP value and Icc2 value in Table 17(DC AND OPERATING CHARACTERISTICS) - Added Synchronous Operating Current(Icc3, Max.40mA) - Added tCSHP(A)(CS high pulse width) parameter as Min.10ns in the ASYNCHRONOUS AC CHARACTERISTICS	September 1, 2004	Preliminary
0.4	Revised - Changed IsB1(< 40°C) and IsBP(3/4 block, < 40°C) from 100μA into 120μA - Changed IsBP(1/2 block and 1/4 block, < 40°C) from 95μA into 115μA	October 12, 2004	Preliminary
1.0	Finalized	January 20, 2005	Final

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4M x 16 bit Synchronous Burst Uni-Transistor CMOS RAM

FEATURES

- Process Technology: CMOS
- Organization: 4M x16 bit
- Power Supply Voltage: 1.7~2.0V
- Three State Outputs
- Supports MRS (Mode Register Set)
- MRS control - MRS Pin Control
- Supports Power Saving modes - Partial Array Refresh mode
Internal TCSR
- Supports Driver Strength Optimization for system environment power saving.
- Supports Asynchronous 4-Page Read and Asynchronous Write Operation
- Supports Synchronous Burst Read and Asynchronous Write Operation(Address Latch Type and Low ADV Type)
- Supports Synchronous Burst Read and Synchronous Burst Write Operation
- Synchronous Burst(Read/Write) Operation
 - Supports 4 word / 8 word / 16 word and Full Page(256 word) burst
 - Supports Linear Burst type & Interleave Burst type
 - Latency support : Latency 5 @ 66MHz(tCD 10ns)
Latency 4 @ 54MHz(tCD 10ns)
 - Supports Burst Read Suspend in No Clock toggling
 - Supports Burst Write Data Masking by /UB & /LB pin control
 - Supports WAIT pin function for indicating data availability.
- Max. Burst Clock Frequency : 66MHz
- Package Type : 54 ball FBGA 6.0mm x 8.0mm

GENERAL DESCRIPTION

The world is moving into the mobile multi-media era and therefore the mobile handsets need much bigger memory capacity to handle the multi-media data.

SAMSUNG's UtRAM products are designed to meet all the request from the various customers who want to cope with the fast growing mobile market.

UtRAM is the perfect solution for the mobile market with its low cost, high density and high performance feature.

K1B6416B6C is fabricated by SAMSUNG's advanced CMOS technology using one transistor memory cell.

The device supports the traditional SRAM like asynchronous bus operation(asynchronous page read and asynchronous write), the NOR flash like synchronous bus operation(synchronous burst read and asynchronous write) and the fully synchronous bus operation(synchronous burst read and synchronous burst write).

These three bus operation modes are defined through the mode register setting.

The device also supports the special features for the standby power saving. Those are the Partial Array Refresh(PAR) mode and internal Temperature Compensated Self Refresh(TCSR) mode.

The optimization of output driver strength is possible through the mode register setting to adjust for the different data loadings.

Through this driver strength optimization, the device can minimize the noise generated on the data bus during read operation.

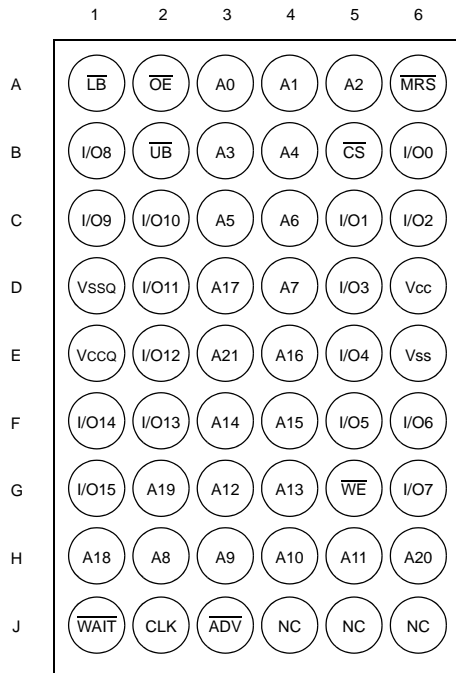
Table 1. PRODUCT FAMILY

Product Family	Operating Temp.	Vcc Range	Clock Freq.(Max)	Async. Speed(tAA)	Current Consumption		
					Standby(Max) (Isb1, <40°C)	Standby(Max) (Isb1, <85°C)	Operating (Icc2, Icc3, Max.)
K1B6416B6C-I	Industrial(-40~85°C)	1.7~2.0V	66MHz	70ns	120µA	180µA	40mA

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Fig.1 PIN DESCRIPTION



54-FBGA: Top View(Ball Down)

Table 2. PIN DESCRIPTION

Name	Function	Name	Function
CLK	Clock Input	I/O0~I/O15	Data Inputs/Outputs
\overline{ADV}	Address Input Valid	Vcc/Vccq	Power Supply
\overline{MRS}	Mode Register set	Vss/Vssq	Ground
\overline{CS}	Chip Select	\overline{UB}	Upper Byte(I/O8~15)
\overline{OE}	Output Enable Input	\overline{LB}	Lower Byte(I/O0~7)
\overline{WE}	Write Enable Input	\overline{WAIT}	Data Availability
A0~A21	Address Inputs	NC	Not Connected

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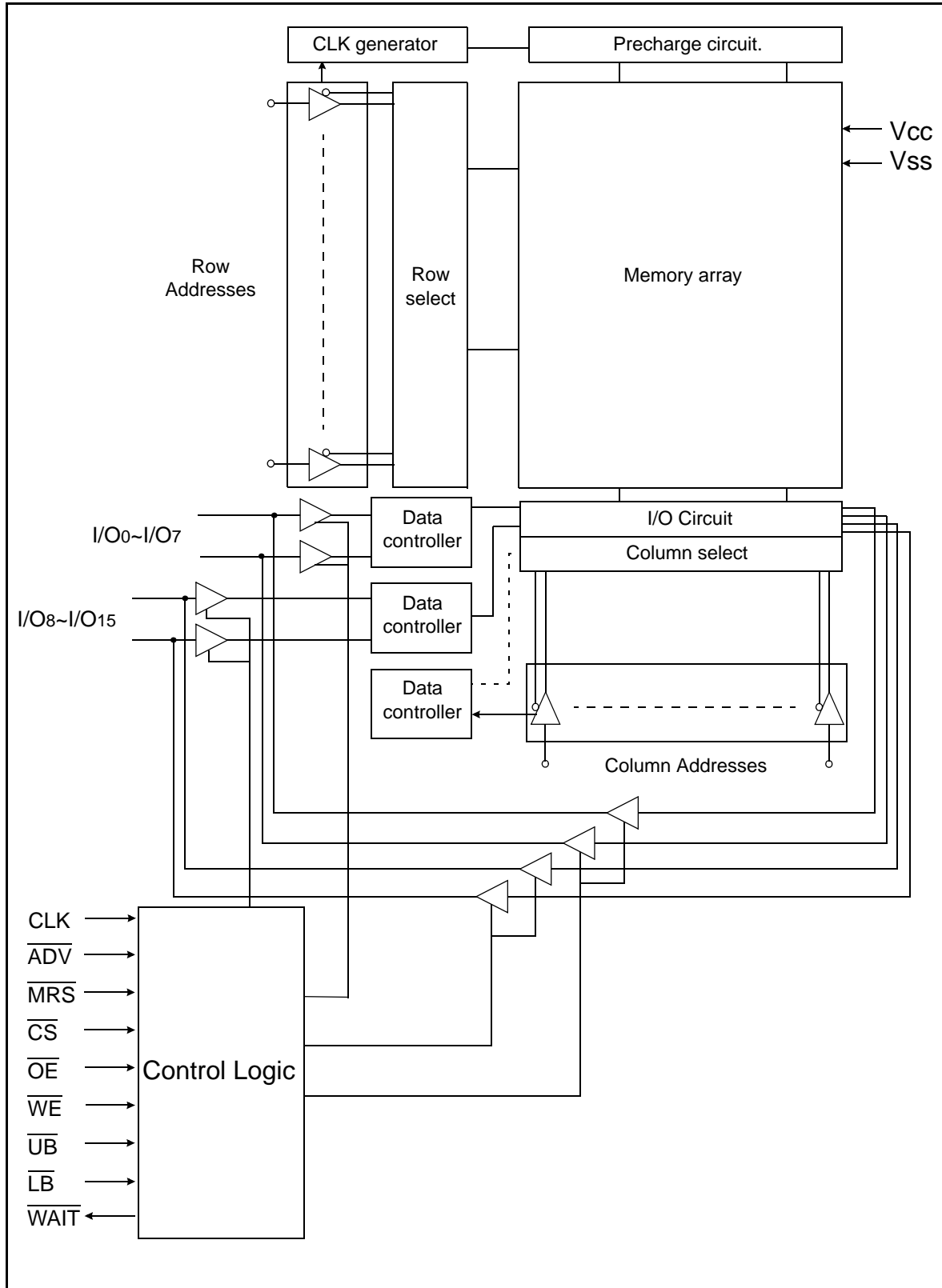
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Fig.2 FUNCTIONAL BLOCK DIAGRAM

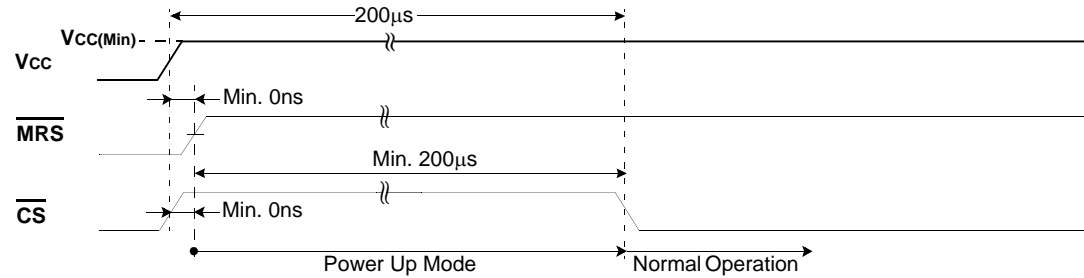


POWER UP SEQUENCE

After applying V_{cc} upto minimum operating voltage(1.7V), drive \overline{CS} High first and then drive \overline{MRS} High. Then the device gets into the Power Up mode. Wait for minimum 200 μ s to get into the normal operation mode. During the Power Up mode, the standby current can not be guaranteed. To get the stable standby current level, at least one cycle of active operation should be implemented regardless of wait time duration. To get the appropriate device operation, be sure to keep the following power up sequence.

1. Apply power.
2. Maintain stable power(V_{cc} min.=1.7V) for a minimum 200 μ s with \overline{CS} and \overline{MRS} high.

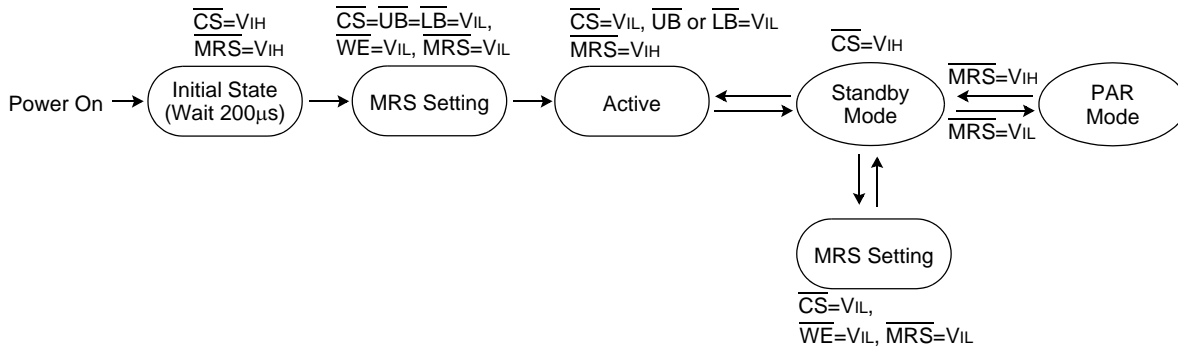
Fig.3 POWER UP TIMING



(Note)

1. After V_{cc} reaches V_{cc(Min)}, wait 200 μ s with \overline{CS} and \overline{MRS} high. Then the device gets into the normal operation.

Fig.4 STANDBY MODE STATE MACHINES



Default mode after power up is Asynchronous mode(4 Page Read and Asynchronous Write). But this default mode is not 100% guaranteed so MRS setting sequence is highly recommended after power up.

For entry to PAR mode, drive \overline{MRS} pin into V_{IL} for over 0.5 μ s(suspend period) during standby mode after MRS setting has been completed(A₄=1, A₃=0). If \overline{MRS} pin is driven into V_{IH} during PAR mode, the device gets back to the standby mode without wake up sequence.

FUNCTIONAL DESCRIPTION

Table 3. ASYNCHRONOUS 4 PAGE READ & ASYNCHRONOUS WRITE MODE(A15/A14=0/0)

\overline{CS}	\overline{MRS}	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	I/O ₀₋₇	I/O ₈₋₁₅	Mode	Power
H	H	X ⁽¹⁾	X ⁽¹⁾	X ⁽¹⁾	X ⁽¹⁾	High-Z	High-Z	Deselected	Standby
H	L	X ⁽¹⁾	X ⁽¹⁾	X ⁽¹⁾	X ⁽¹⁾	High-Z	High-Z	Deselected	PAR
L	H	H	H	X ⁽¹⁾	X ⁽¹⁾	High-Z	High-Z	Output Disabled	Active
L	H	X ⁽¹⁾	X ⁽¹⁾	H	H	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	H	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	H	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	H	L	L	L	Din	Din	Word Write	Active
L	L	H	L	L	L	High-Z	High-Z	Mode Register Set	Active

1. X must be low or high state.
2. In asynchronous mode, Clock and \overline{ADV} are ignored.
3. /WAIT pin is High-Z in Asynchronous mode.

Table 4. SYNCHRONOUS BURST READ & ASYNCHRONOUS WRITE MODE(A15/A14=0/1)

\overline{CS}	\overline{MRS}	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	I/O ₀₋₇	I/O ₈₋₁₅	CLK	\overline{ADV}	Mode	Power
H	H	X ⁽¹⁾	X ⁽¹⁾	X ⁽¹⁾	X ⁽¹⁾	High-Z	High-Z	X ⁽²⁾	X ⁽²⁾	Deselected	Standby
H	L	X ⁽¹⁾	X ⁽¹⁾	X ⁽¹⁾	X ⁽¹⁾	High-Z	High-Z	X ⁽²⁾	X ⁽²⁾	Deselected	PAR
L	H	H	H	X ⁽¹⁾	X ⁽¹⁾	High-Z	High-Z	X ⁽²⁾	H	Output Disabled	Active
L	H	X ⁽¹⁾	X ⁽¹⁾	H	H	High-Z	High-Z	X ⁽²⁾	H	Output Disabled	Active
L	H	X ⁽¹⁾	H	X ⁽¹⁾	X ⁽¹⁾	High-Z	High-Z			Read Command	Active
L	H	L	H	L	H	Dout	High-Z		H	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout		H	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout		H	Word Read	Active
L	H	H	L	L	H	Din	High-Z	X ⁽²⁾		Lower Byte Write	Active
L	H	H	L	H	L	High-Z	Din	X ⁽²⁾		Upper Byte Write	Active
L	H	H	L	L	L	Din	Din	X ⁽²⁾		Word Write	Active
L	L	H	L	L	L	High-Z	High-Z	X ⁽²⁾		Mode Register Set	Active

1. X must be low or high state.
2. X means "Don't care"(can be low, high or toggling).
3. /WAIT is device output signal so does not have any affect to the mode definition. Please refer to each timing diagram for /WAIT pin function.

Table 5. SYNCHRONOUS BURST READ & SYNCHRONOUS BURST WRITE MODE(A15/A14=1/0)

$\overline{\text{CS}}$	$\overline{\text{MRS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{LB}}$	$\overline{\text{UB}}$	I/O ₀₋₇	I/O ₈₋₁₅	CLK	$\overline{\text{ADV}}$	Mode	Power
H	H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	X ²⁾	X ²⁾	Deselected	Standby
H	L	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	X ²⁾	X ²⁾	Deselected	PAR
L	H	H	H	X ¹⁾	X ¹⁾	High-Z	High-Z	X ²⁾	H	Output Disabled	Active
L	H	X ¹⁾	X ¹⁾	H	H	High-Z	High-Z	X ²⁾	H	Output Disabled	Active
L	H	X ¹⁾	H	X ¹⁾	X ¹⁾	High-Z	High-Z			Read Command	Active
L	H	L	H	L	H	Dout	High-Z		H	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout		H	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout		H	Word Read	Active
L	H	X ¹⁾	L or	X ¹⁾	X ¹⁾	High-Z	High-Z			Write Command	Active
L	H	H	X ¹⁾	L	H	Din	High-Z		H	Lower Byte Write	Active
L	H	H	X ¹⁾	H	L	High-Z	Din		H	Upper Byte Write	Active
L	H	H	X ¹⁾	L	L	Din	Din		H	Word Write	Active
L	L	H	L or	L	L	High-Z	High-Z			Mode Register Set	Active

1. X must be low or high state.

2. X means "Don't care"(can be low, high or toggling).

3. /WAIT is device output signal so does not have any affect to the mode definition. Please refer to each timing diagram for /WAIT pin function.

4. The last data written in the previous Asynchronous write mode is not valid. To make the lastly written data valid, then implement at least one dummy write cycle before change mode into synchronous burst read and synchronous burst write mode.

5. The data written in Synchronous burst write operation can be corrupted by the next Asynchronous write operation. So the transition from Synchronous burst write operation to Asynchronous write operation is prohibited.

MODE REGISTER SETTING OPERATION

The device has several modes : Asynchronous Page Read mode, Asynchronous Write mode, Synchronous Burst Read mode, Synchronous Burst Write mode, Standby mode and Partial Array Refresh(PAR) mode.

Partial Array Refresh(PAR) mode is defined through Mode Register Set(MRS) option. Mode Register Set(MRS) option also defines Burst Length, Burst Type, Wait Polarity and Latency Count at Synchronous Burst Read/Write mode.

Mode Register Set (MRS)

The mode register stores the data for controlling the various operation modes of UtRAM. It programs Partial Array Refresh(PAR), Burst Length, Burst Type, Latency Count and various vendor specific options to make UtRAM useful for a variety of different applications. The default values of mode register are defined, therefore when the reserved address is input, the device runs at default modes. The mode register is written by driving CS, ADV, WE, UB, LB and MRS to VIL and driving OE to VIH during valid address. The mode register is divided into various fields depending on the fields of functions. The Partial Array Refresh(PAR) field uses A0~A4, Burst Length field uses A5~A7, Burst Type uses A8, Latency Count uses A9~A11, Wait Polarity uses A13, Operation Mode uses A14~A15 and Driver Strength uses A16~A17.

Refer to the Table below for detailed Mode Register Setting. A18~A21 addresses are "Don't care" in Mode Register Setting.

Table 6. Mode Register Setting according to field of function

Address	A17~A16	A15~A14	A13	A12	A11~A9	A8	A7~A5	A4~A3	A2	A1~A0
Function	DS	MS	WP	RFU	Latency	BT	BL	PAR	PARA	PARS

NOTE : DS(Driver Strength), MS(Mode Select), WP(Wait Polarity), Latency(Latency Count), BT(Burst Type), BL(Burst Length), PAR(Partial Array Refresh), PARA(Partial Array Refresh Array), PARS(Partial Array Refresh Size), RFU(Reserved for Future Use)

Table 7. Mode Register Set

Driver Strength			Mode Select			
A17	A16	DS	A15	A14	MS*	
0	0	Full Drive	0	0	Async. 4 Page Read / Async. Write	
0	1	1/2 Drive	0	1	Sync. Burst Read / Async. Write	
1	0	1/4 Drive	1	0	Sync. Burst Read / Sync. Burst Write	

WAIT Polarity		RFU		Latency Count				Burst Type		Burst Length			
A13	WP	A12	RFU	A11	A10	A9	Latency	A8	BT	A7	A6	A5	BL
0	Low Enable	0	Must	0	0	0	3	0	Linear	0	1	0	4 word
1	High Enable	1	-	0	0	1	4	1	Interleave	0	1	1	8 word
				0	1	0	5			1	0	0	16 word
				0	1	1	6			1	1	1	Full(256 word)

Partial Array Refresh			PAR Array		PAR Size		
A4	A3	PAR	A2	PARA	A1	A0	PARS
1	0	PAR Enable	0	Bottom Array	0	0	Full Array
1	1	PAR Disable	1	Top Array	0	1	3/4 Array
					1	0	1/2 Array
					1	1	1/4 Array

NOTE : The address bits other than those listed in the table above are reserved.

For example, Burst Length address bits(A7:A6:A5) have 4 sets of reserved bits like 0:0:0, 0:0:1, 1:0:1 and 1:1:0.

If the reserved address bits are input, then the mode will be set into the default mode. Each field has its own default mode and these default modes are written in blue-bold in the table above.

But this default mode is not 100% guaranteed so MRS setting sequence is highly recommended after power up.

A12 is a reserved bit for future use. A12 must be set as "0".

Not all the mode settings are tested. Per the mode settings to be tested, please contact Samsung Product Planning team. **256 word Full page burst mode needs to meet tBC(Burst Cycle time) parameter as max. 2500ns.**

* The last data written in the previous Asynchronous write mode is not valid. To make the lastly written data valid, then implement at least one dummy write cycle before change mode into synchronous burst read and synchronous burst write mode.

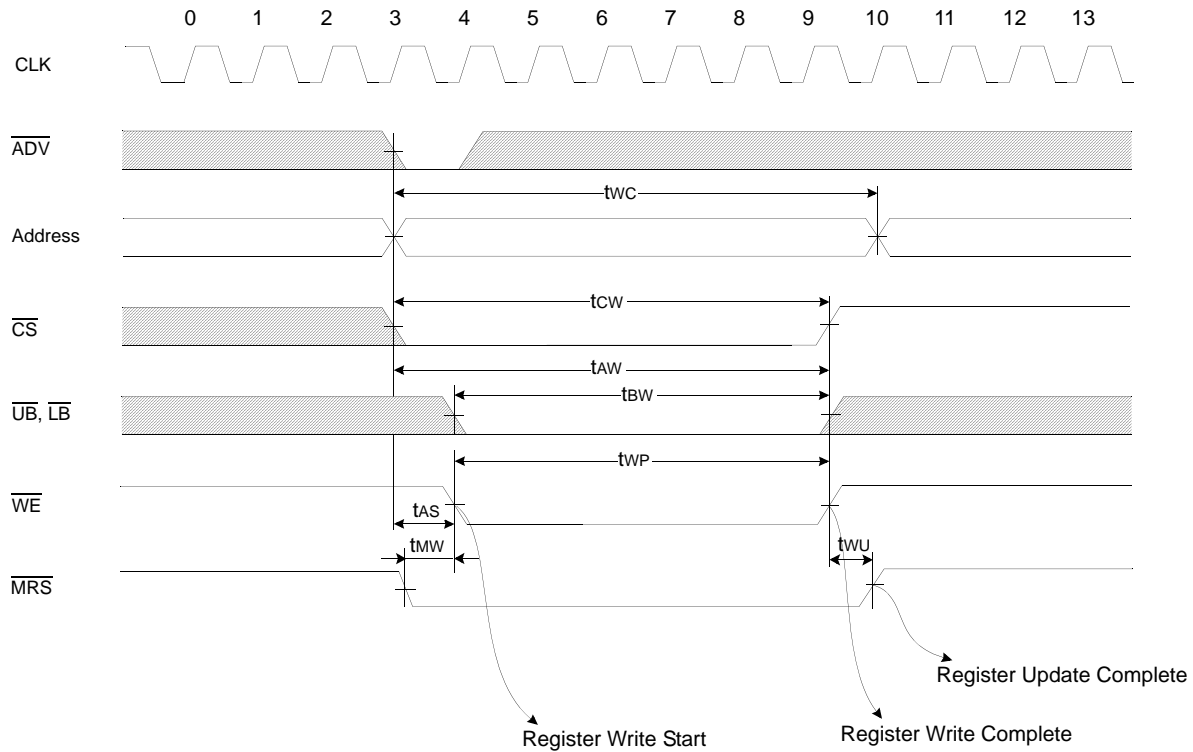
* The data written in Synchronous burst write operation can be corrupted by the next Asynchronous write operation. So the transition from Synchronous burst write operation to Asynchronous write operation is prohibited.

MRS pin Control Type Mode Register Setting Timing

In this device(K1B6416B6C), MRS pin is used for two purposes. One is to get into the mode register setting and the other one is to execute Partial Array Refresh mode.

To get into the Mode Register Setting, the system must drive $\overline{\text{MRS}}$ pin to V_{IL} and immediately(within 0.5 μs) issue a write command(drive CS, ADV, UB, LB and WE to V_{IL} and drive OE to V_{IH} during valid address). If the subsequent write command(WE signal input) is not issued within 0.5 μs , then the device might get into the PAR mode.

Fig.5 MODE REGISTER SETTING TIMING($\overline{\text{OE}}=V_{IH}$)



(MRS SETTING TIMING)
1. Clock input is ignored.

Table 8. MRS AC CHARACTERISTICS ($V_{CC}=1.7\sim 2.0V$, $T_A=-40$ to 85°C , Maximum Main Clock Frequency=66MHz)

Parameter List		Symbol	Speed		Units
			Min	Max	
MRS	$\overline{\text{MRS}}$ Enable to Register Write Start	t_{MW}	0	500	ns
	End of Write to $\overline{\text{MRS}}$ Disable	t_{WU}	0	-	ns

ASYNCHRONOUS OPERATION

Asynchronous 4 Page Read Operation

Asynchronous normal read operation starts when \overline{CS} , \overline{OE} and \overline{UB} or \overline{LB} are driven to V_{IL} under the valid address without toggling page addresses(A0, A1). If the page addresses(A0, A1) are toggled under the other valid address, the first data will be out with the normal read cycle time(tRC) and the second, the third and the fourth data will be out with the page cycle time(tPC). (MRS and WE should be driven to V_{IH} during the asynchronous (page) read operation) Clock, ADV, WAIT signals are ignored during the asynchronous (page) read operation.

Asynchronous Write Operation

Asynchronous write operation starts when \overline{CS} , \overline{WE} and \overline{UB} or \overline{LB} are driven to V_{IL} under the valid address. (MRS and \overline{OE} should be driven to V_{IH} during the asynchronous write operation.) Clock, ADV, WAIT signals are ignored during the asynchronous (page) read operation.

Asynchronous Write Operation in Synchronous Mode

A write operation starts when \overline{CS} , \overline{WE} and \overline{UB} or \overline{LB} are driven to V_{IL} under the valid address. Clock input does not have any affect to the write operation(MRS and \overline{OE} should be driven to V_{IH} during write operation. ADV can be either toggling for address latch or held in V_{IL}). Clock, ADV, WAIT signals are ignored during the asynchronous (page) read operation.

Fig.6 ASYNCHRONOUS 4-PAGE READ

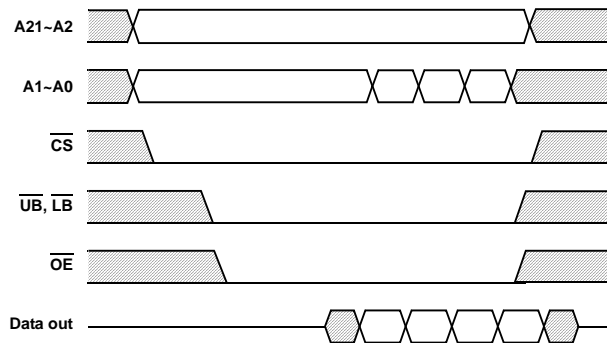
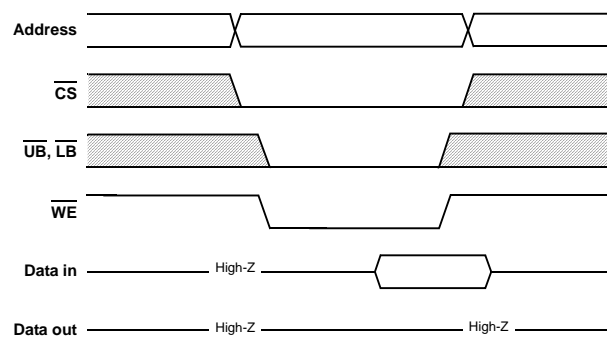


Fig.7 ASYNCHRONOUS WRITE



SYNCHRONOUS BURST OPERATION

Burst mode operations enable the system to get high performance read and write operation. The address to be accessed is latched on the rising edge of clock or ADV (whichever occurs first). CS should be setup before the address latch. During this first clock rising edge, WE indicates whether the operation is going to be a Read (WE High) or a Write (WE Low). For the optimized Burst Mode to each system, the system should determine how many clock cycles are required for the first data of each burst access (Latency Count), how many words the device outputs at an access (Burst Length) and which type of burst operation (Burst Type : Linear or Interleave) is needed. The Wait Polarity should also be determined. (See Table "Mode Register Set")

Synchronous Burst Read Operation

The Synchronous Burst Read command is implemented when the clock rising is detected during the ADV low pulse. ADV and CS should be set up before the clock rising. During Read command, WE should be held in V_{IH} . The multiple clock risings (during low ADV period) are allowed but the burst operation starts from the first clock rising. The first data will be out with Latency count and tCD.

Synchronous Burst Write Operation

The Synchronous Burst Write command is implemented when the clock rising is detected during the ADV and WE low pulse. ADV, WE and CS should be set up before the clock rising. The multiple clock risings (during low ADV period) are allowed but the burst operation starts from the first clock rising. The first data will be written in the Latency clock with tDS.

Fig.8 SYNCHRONOUS BURST READ (Latency 5, BL 4, WP : Low Enable)

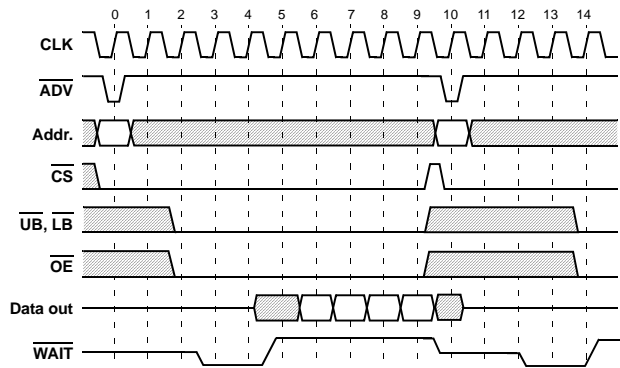
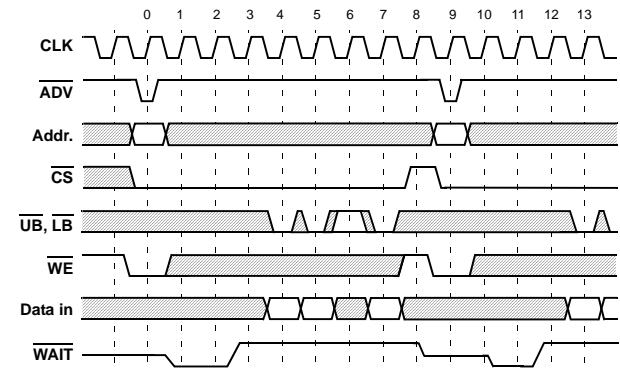


Fig.9 SYNCHRONOUS BURST WRITE (Latency 5, BL 4, WP : Low Enable)



SYNCHRONOUS BURST OPERATION TERMINOLOGY

Clock(CLK)

The clock input is used as the reference for synchronous burst read and write operation of U τ RAM. The synchronous burst read and write operation is synchronized to the rising edge of the clock. The clock transitions must swing between V_{IL} and V_{IH}.

Latency Count

The Latency Count configuration tells the device how many clocks must elapse from the burst command before the first data should be available on its data pins. This value depends on the input clock frequency. The supported Latency Count is as follows.

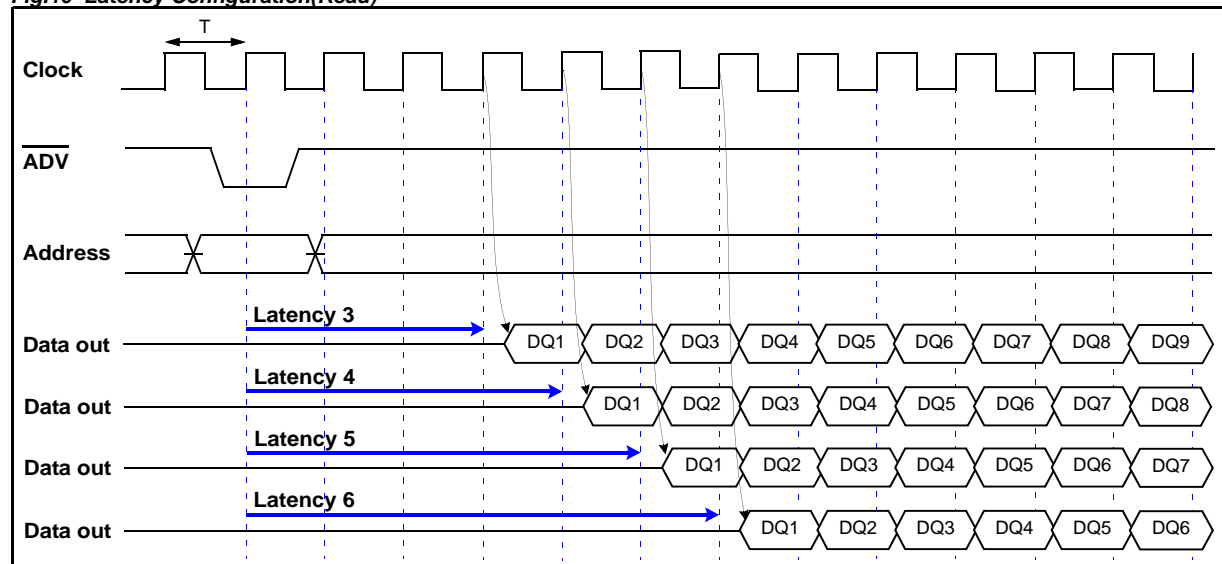
Table 9. Latency Count support : 3, 4, 5

Clock Frequency	Upto 66MHz	Upto 54MHz	Upto 40MHz
Latency Count	5	4	3

Table 10. Number of Clocks for 1st Data

Set Latency	Latency 3	Latency 4	Latency 5
# of Clocks for 1st data(Read)	4	5	6
# of Clocks for 1st data(Write)	2	3	4

Fig.10 Latency Configuration(Read)



NOTE : The first data will always keep the Latency. From the second data, some period of wait time might be caused by WAIT pin.

Burst Length

Burst Length identifies how many data the device outputs at an access. The device supports 4 word, 8 word, 16 word and 256 word burst read or write. 256 word Full page burst mode needs to meet tBC(Burst Cycle time) parameter as max. 2500ns. The first data will be out with the set Latency + tCD. From the second data, the data will be out with tCD from each clock.

Burst Stop

Burst stop is used when the system wants to stop burst operation on special purpose. If driving \overline{CS} to V_{IH} during the burst read operation, then the burst operation will be stopped. During the burst read operation, the new burst operation can not be issued. The new burst operation can be issued only after the previous burst operation is finished.

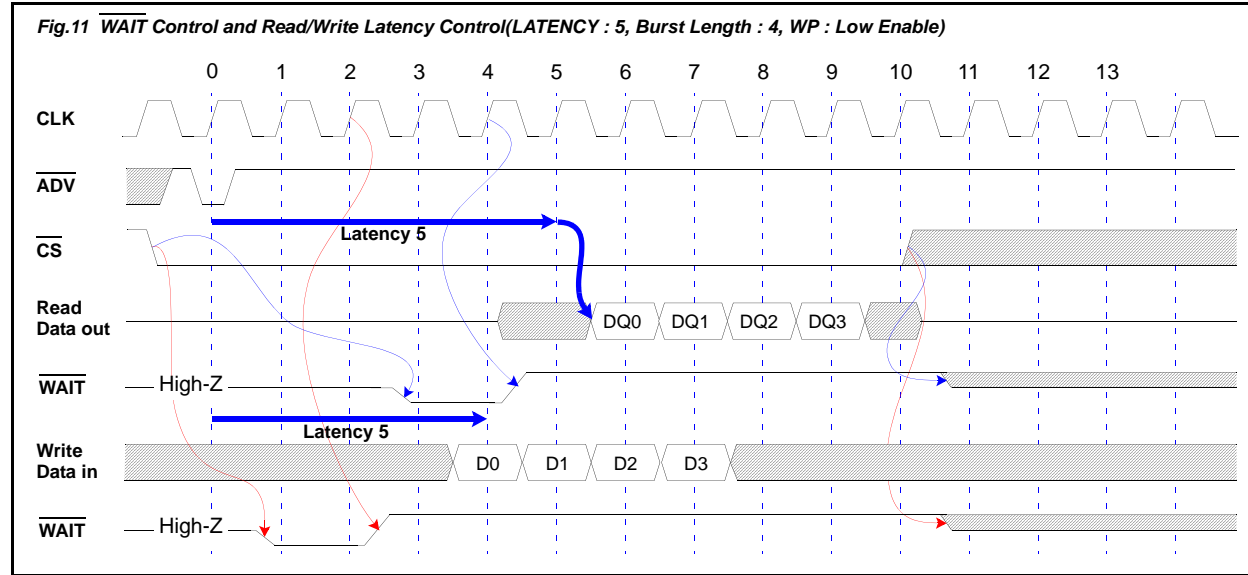
The burst stop feature is very useful because it enables the user to utilize the un-supported burst length such as 1 burst or 2 burst which accounts for big portion in usage for the mobile handset application environment.

SYNCHRONOUS BURST OPERATION TERMINOLOGY

WAIT Control($\overline{\text{WAIT}}$)

The $\overline{\text{WAIT}}$ signal is the device's output signal which indicates to the host system when the device's data-out or data-in is valid. To be compatible with the Flash interfaces of various microprocessor types, the WAIT polarity(WP) can be configured. The polarity can be programmed to be either low enable or high enable.

For the timing of $\overline{\text{WAIT}}$ signal, the $\overline{\text{WAIT}}$ signal should be set active one clock prior to the data regardless of Read or Write cycle.



Burst Type

The device supports Linear type burst sequence and Interleave type burst sequence. Linear type burst sequentially increments the burst address from the starting address. The detailed Linear and Interleave type burst address sequence is shown in burst sequence table in next page.

Table 11. Burst Sequence

Start Addr.	Burst Address Sequence(Decimal)						
	Wrap ¹⁾						
	4 word Burst		8 word Burst		16 word Burst		Full Page(256 word)
Linear	Interleave	Linear	Interleave	Linear	Interleave	Linear	
0	0-1-2-3	0-1-2-3	0-1-...-5-6-7	0-1-2-...-6-7	0-1-2-...-14-15	0-1-2-3-4...14-15	0-1-2-...-254-255
1	1-2-3-0	1-0-3-2	1-2-...-6-7-0	1-0-3-...-7-6	1-2-3-...-15-0	1-0-3-2-5...15-14	1-2-3-...-255-0
2	2-3-0-1	2-3-0-1	2-3-...-7-0-1	2-3-0-...-4-5	2-3-4-...-0-1	2-3-0-1-6...12-13	2-3-4-...-255-0-1
3	3-0-1-2	3-2-1-0	3-4-...-0-1-2	3-2-1-...-5-4	3-4-5-...-1-2	3-2-1-0-7...13-12	3-4-5-...-255-0-1-2
4			4-5-...-1-2-3	4-5-6-...-2-3	4-5-6-...-2-3	4-5-6-7-0...10-11	4-5-6-...-255-0-1-2-3
5			5-6-...-2-3-4	5-4-7-...-3-2	5-6-7-...-3-4	5-4-7-6-1...11-10	5-6-7-...-255-...-3-4
6			6-7-...-3-4-5	6-7-4-...-0-1	6-7-8-...-4-5	6-7-4-5-2...8-9	6-7-8-...-255-...-4-5
7			7-0-...-4-5-6	7-6-5-...-1-0	7-8-9-...-5-6	7-6-5-4-3...9-8	7-8-9-...-255-...-5-6
~					~	~	~
14					14-15-0-...-12-13	14-15-12-...-0-1	14-15-...-255-...-12-13
15					15-0-1-...-13-14	15-14-13-...-1-0	15-16-...-255-...-13-14
~							~
255							255-0-1-...-253-254

1. Wrap : Burst Address wraps within word boundary and ends after fulfilled the burst length.

2. 256 word Full page burst mode needs to meet t_{BC}(Burst Cycle time) parameter as max. 2500ns.

LOW POWER FEATURES

Partial Array Refresh(PAR) mode

The PAR mode enables the user to specify the active memory array size. UtRAM consists of 4 blocks and user can select 1 block, 2 blocks, 3 blocks or all blocks as active memory array through Mode Register Setting. The active memory array is periodically refreshed whereas the disabled array is not going to be refreshed and so the previously stored data will get lost. Even though PAR mode is enabled through the Mode Register Setting, PAR mode execution by MRS pin is still needed. The normal operation can be executed even in refresh-disabled array as long as MRS pin is not driven to low for over 0.5μs. Driving MRS pin to high makes the device to get back to the normal operation mode from PAR executed mode, Refer to Fig.13 and Table 12 for PAR operation and PAR address mapping.

Driver Strength Optimization

The optimization of output driver strength is possible through the mode register setting to adjust for the different data loadings. Through this driver strength optimization, the device can minimize the noise generated on the data bus during read operation. The device supports full drive, 1/2 drive and 1/4 drive.

Internal TCSR

The internal Temperature Compensated Self Refresh(TCSR) feature is a very useful tool for reducing standby current in room temperature(below 40°C). DRAM cell has weak refresh characteristics in higher temperature. So high temperature requires more refresh cycles, which lead to standby current increase. Without internal TCSR, the refresh cycle should be set as worst condition so as to cover high temperature(85°C) refresh characteristics. But with internal TCSR, the refresh cycle below 40°C can be optimized, so the standby current in room temperature can be highly reduced. This feature is really beneficial to mobile phone because most of mobile phones are used at below 40°C in the phone standby mode.

Fig.13 PAR MODE EXECUTION and EXIT

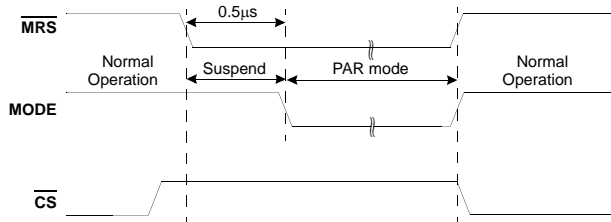


Table 12. PAR MODE CHARACTERISTIC

Power Mode	Address (Bottom Array) ²⁾	Address (Top Array) ²⁾	Memory Cell Data	Standby ³⁾ (ISB1, <40°C)	Standby ³⁾ (ISB1, <85°C)	Wait Time(μs)
Standby(Full Array)	000000h ~ 3FFFFFFh	000000h ~ 3FFFFFFh	Valid ¹⁾	120μA	180μA	0
Partial Refresh(3/4 Block)	000000h ~ 2FFFFFFh	100000h ~ 3FFFFFFh	Valid ¹⁾	120μA	180μA	0
Partial Refresh(1/2 Block)	000000h ~ 1FFFFFFh	200000h ~ 3FFFFFFh	Valid ¹⁾	115μA	165μA	0
Partial Refresh(1/4 Block)	000000h ~ 0FFFFFFh	300000h ~ 3FFFFFFh	Valid ¹⁾	115μA	165μA	0

1. Only the data in the refreshed block are valid
2. PAR Array can be selected through Mode Register Set(See Page 11)
3. Standby mode is supposed to be set up after at least one active operation.after power up.
ISB1 is measured after 60ms from the time when standby mode is set up.

Table 13. PRODUCT LIST

Industrial Temperature Products(-40~85°C)	
Part Name	Function
K1B6416B6C	1.8V, 70ns, 66MHz

Table 14. ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.2 to V _{CC} +0.3V	V
Power supply voltage relative to Vss	V _{CC}	-0.2 to 2.5V	V
Power Dissipation	P _D	1.0	W
Storage temperature	T _{STG}	-65 to 150	°C
Operating Temperature	T _A	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

Table 15. RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V _{CC}	1.7	1.85	2.0	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	0.8 x V _{CC}	-	V _{CC} +0.2 ²⁾	V
Input low voltage	V _{IL}	-0.2 ³⁾	-	0.4	V

1. T_A=-40 to 85°C, otherwise specified.
2. Overshoot: V_{CC}+1.0V in case of pulse width ≤20ns.
3. Undershoot: -1.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

Table 16. CAPACITANCE¹⁾(f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

Table 17. DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit		
Input Leakage Current	I _{LI}	V _{IN} =V _{SS} to V _{CCQ}	-1	-	1	μA		
Output Leakage Current	I _{LO}	$\overline{CS}=V_{IH}$, $\overline{MRS}=V_{IH}$, $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CCQ}	-1	-	1	μA		
Average Operating Current(Async)	I _{CC2}	Cycle time=t _{RC} +3t _{PC} , I _{IO} =0mA, 100% duty, $\overline{CS}=V_{IL}$, $\overline{MRS}=V_{IH}$, V _{IN} =V _{IL} or V _{IH}	-	-	40	mA		
Average Operating Current(Sync)	I _{CC3}	Burst Length 4, Latency 5, 66MHz, I _{IO} =0mA, Address transition 1 time, $\overline{CS}=V_{IL}$, $\overline{MRS}=V_{IH}$, V _{IN} =V _{IL} or V _{IH}	-	-	40	mA		
Output Low Voltage	V _{OL}	I _{OL} =0.1mA	-	-	0.2	V		
Output High Voltage	V _{OH}	I _{OH} =-0.1mA	1.4	-	-	V		
Standby Current(CMOS)	I _{SB1} ²⁾	$\overline{CS} \geq V_{CCQ}-0.2V$, $\overline{MRS} \geq V_{CCQ}-0.2V$, Other inputs=V _{SS} to V _{CCQ}	< 40°C	-	-	120	μA	
			< 85°C	-	-	180	μA	
Partial Refresh Current	I _{SBP} ¹⁾	$\overline{MRS} \leq 0.2V$, $\overline{CS} \geq V_{CCQ}-0.2V$ Other inputs=V _{SS} to V _{CCQ}	< 40°C	3/4 Block	-	-	120	μA
				1/2 Block	-	-	115	
				1/4 Block	-	-	115	
			< 85°C	3/4 Block	-	-	180	μA
				1/2 Block	-	-	165	
				1/4 Block	-	-	165	

1. Full Array Partial Refresh Current(I_{SBP}) is same as Standby Current(I_{SB1}).

2. Standby mode is supposed to be set up after at least one active operation after power up.

I_{SB1} is measured after 60ms from the time when standby mode is set up.

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Test Input/Output Reference)

Input pulse level: 0.2 to V_{cc}-0.2V
 Input rising and falling time: 3ns
 Input and output reference voltage: 0.5 x V_{cc}
 Output load: C_L=30pF

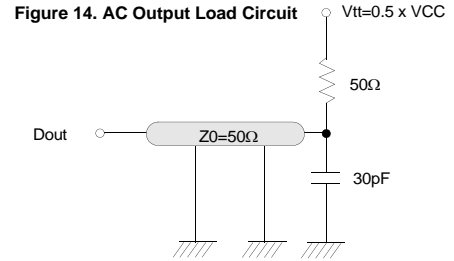


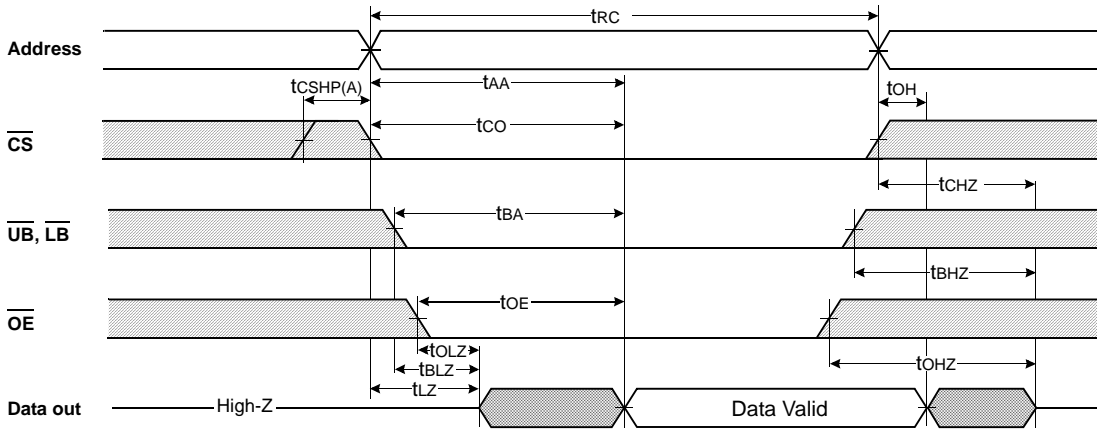
Table 18. ASYNCHRONOUS AC CHARACTERISTICS (V_{CC}=1.7~2.0V, T_A=-40 to 85°C)

	Parameter List	Symbol	Speed		Units
			Min	Max	
Common	\overline{CS} High Pulse Width	tCSHP(A)	10	-	ns
Async. (Page) Read	Read Cycle Time	tRC	70	-	ns
	Page Read Cycle Time	tPC	25	-	ns
	Address Access Time	tAA	-	70	ns
	Page Access Time	tPA	-	20	ns
	Chip Select to Output	tCO	-	70	ns
	Output Enable to Valid Output	tOE	-	35	ns
	\overline{UB} , \overline{LB} Access Time	tBA	-	35	ns
	Chip Select to Low-Z Output	tLZ	10	-	ns
	\overline{UB} , \overline{LB} Enable to Low-Z Output	tBLZ	5	-	ns
	Output Enable to Low-Z Output	tOLZ	5	-	ns
	Chip Disable to High-Z Output	tCHZ	0	12	ns
	\overline{UB} , \overline{LB} Disable to High-Z Output	tBHZ	0	12	ns
	Output Disable to High-Z Output	tOHZ	0	12	ns
	Output Hold	tOH	3	-	ns
Async. Write	Write Cycle Time	tWC	70	-	ns
	Chip Select to End of Write	tCW	60	-	ns
	\overline{ADV} Minimum Low Pulse Width	tADV	7	-	ns
	Address Set-up Time to Beginning of Write	tAS	0	-	ns
	Address Set-up Time to \overline{ADV} Falling	tAS(A)	0	-	ns
	Address Hold Time from \overline{ADV} Rising	tAH(A)	7	-	ns
	\overline{CS} Setup Time to \overline{ADV} Rising	tCSS(A)	10	-	ns
	Address Valid to End of Write	tAW	60	-	ns
	\overline{UB} , \overline{LB} Valid to End of Write	tBW	60	-	ns
	Write Pulse Width	tWP	55 ¹⁾	-	ns
	\overline{WE} High Pulse Width	tWHP	5 ns	Latency-1 clock	-
	Write Recovery Time	tWR	0	-	ns
	\overline{WE} Low to Read Latency	tWLRL	1	-	clock
	Data to Write Time Overlap	tDW	30	-	ns
Data Hold from Write Time	tDH	0	-	ns	

1. tWP(min)=70ns for continuous write operation over 50 times.

ASYNCHRONOUS READ TIMING WAVEFORM

Fig.15 TIMING WAVEFORM OF ASYNCHRONOUS READ CYCLE ($\overline{MRS}=V_{IH}$, $\overline{WE}=V_{IH}$, $\overline{WAIT}=High-Z$)



(ASYNCHRONOUS READ CYCLE)

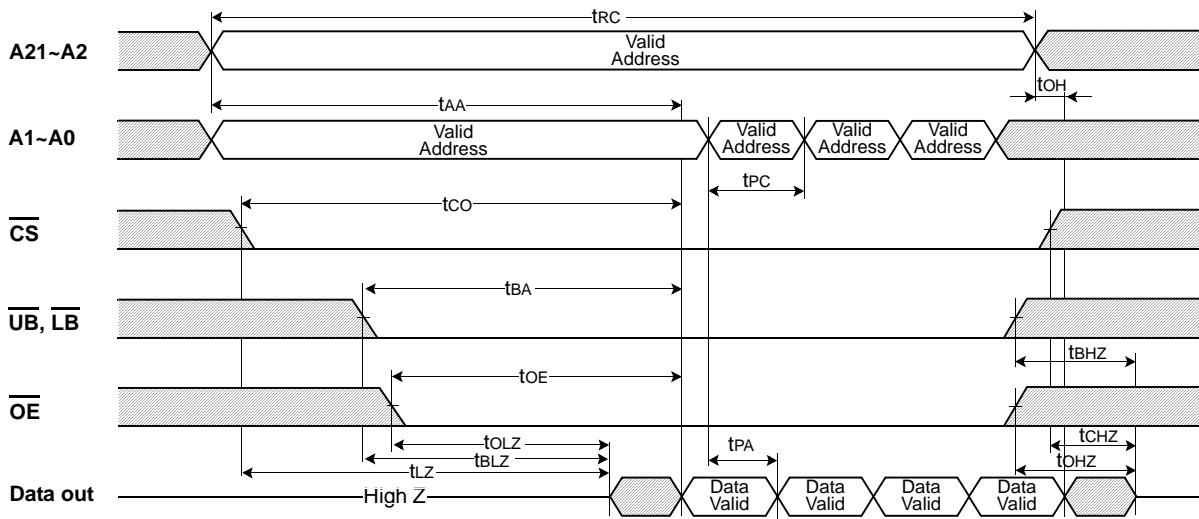
1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{CHZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.
3. In asynchronous read cycle, Clock, \overline{ADV} and \overline{WAIT} signals are ignored.

Table 19. ASYNCHRONOUS READ AC CHARACTERISTICS

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
t_{RC}	70	-	ns	t_{OLZ}	5	-	ns
t_{AA}	-	70	ns	t_{BLZ}	5	-	ns
t_{CO}	-	70	ns	t_{LZ}	10	-	ns
t_{BA}	-	35	ns	t_{CHZ}	0	12	ns
t_{OE}	-	35	ns	t_{BHZ}	0	12	ns
t_{OH}	3	-	ns	t_{OHZ}	0	12	ns
$t_{CSHP(A)}$	10	-	ns				

ASYNCHRONOUS READ TIMING WAVEFORM

Fig.16 TIMING WAVEFORM OF PAGE READ CYCLE ($\overline{MRS}=V_{IH}$, $\overline{WE}=V_{IH}$, $\overline{WAIT}=\text{High-Z}$)



(ASYNCHRONOUS 4 PAGE READ CYCLE)

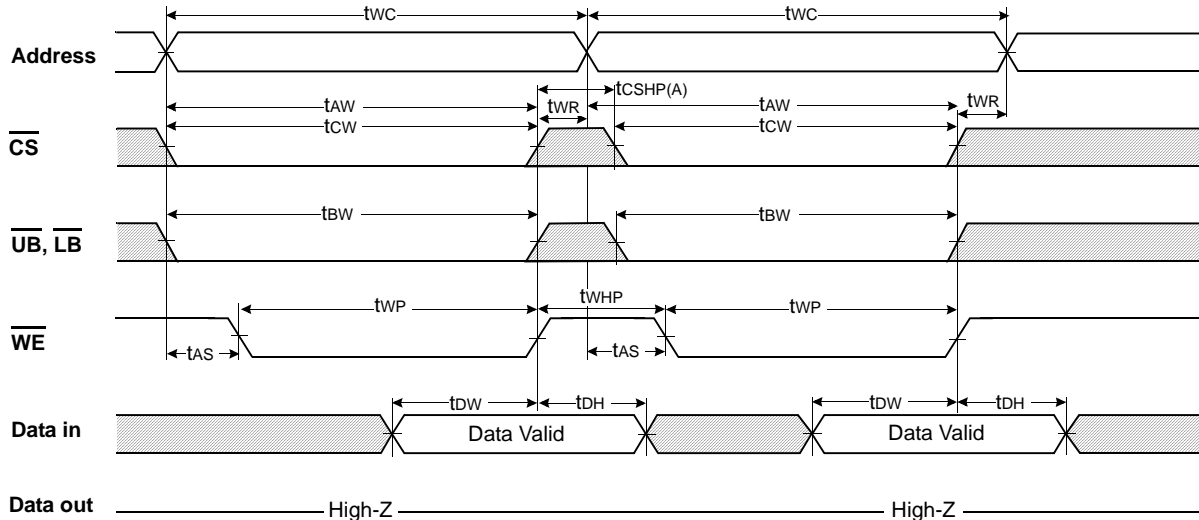
1. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{CHZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.
3. In asynchronous 4 page read cycle, Clock, \overline{ADV} and \overline{WAIT} signals are ignored.

Table 20. ASYNCHRONOUS PAGE READ AC CHARACTERISTICS

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
t_{RC}	70	-	ns	t_{OH}	3	-	ns
t_{AA}	-	70	ns	t_{OLZ}	5	-	ns
t_{PC}	25	-	ns	t_{BLZ}	5	-	ns
t_{PA}	-	20	ns	t_{LZ}	10	-	ns
t_{CO}	-	70	ns	t_{CHZ}	0	12	ns
t_{BA}	-	35	ns	t_{BHZ}	0	12	ns
t_{OE}	-	35	ns	t_{OHZ}	0	12	ns

ASYNCHRONOUS WRITE TIMING WAVEFORM

Fig.17 TIMING WAVEFORM OF WRITE CYCLE(1)($\overline{MRS}=V_{IH}, \overline{OE}=V_{IH}, \overline{WAIT}=\text{High-Z}, \overline{WE}$ Controlled)



(ASYNCHRONOUS WRITE CYCLE - \overline{WE} Controlled)

1. A write occurs during the overlap (t_{WP}) of low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when \overline{CS} goes high or \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS} going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with \overline{CS} or \overline{WE} going high.
5. In asynchronous write cycle, Clock, ADV and WAIT signals are ignored.
6. Condition for continuous write operation over 50 times : $t_{WP}(\text{min})=70\text{ns}$

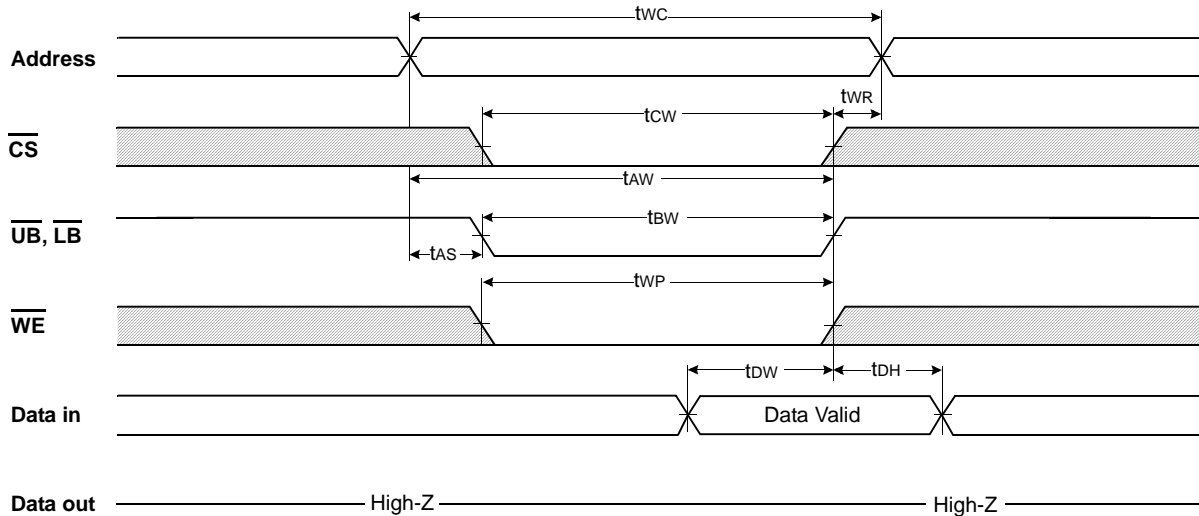
Table 21. ASYNCHRONOUS WRITE AC CHARACTERISTICS (\overline{WE} Controlled)

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
t_{WC}	70	-	ns	t_{AS}	0	-	ns
t_{CW}	60	-	ns	t_{WR}	0	-	ns
t_{AW}	60	-	ns	t_{DW}	30	-	ns
t_{BW}	60	-	ns	t_{DH}	0	-	ns
t_{WP}	55 ¹⁾	-	ns	$t_{CSHP(A)}$	10	-	ns

1. $t_{WP}(\text{min})=70\text{ns}$ for continuous write operation over 50 times.

ASYNCHRONOUS WRITE TIMING WAVEFORM

Fig.18 TIMING WAVEFORM OF WRITE CYCLE(2)($\overline{MRS}=V_{IH}$, $\overline{OE}=V_{IH}$, $\overline{WAIT}=\text{High-Z}$, \overline{UB} & \overline{LB} Controlled)



(ASYNCHRONOUS WRITE CYCLE - \overline{UB} & \overline{LB} Controlled)

1. A write occurs during the overlap(t_{WP}) of low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when \overline{CS} goes high or \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS} going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with \overline{CS} or \overline{WE} going high.
5. In asynchronous write cycle, Clock, \overline{ADV} and \overline{WAIT} signals are ignored.

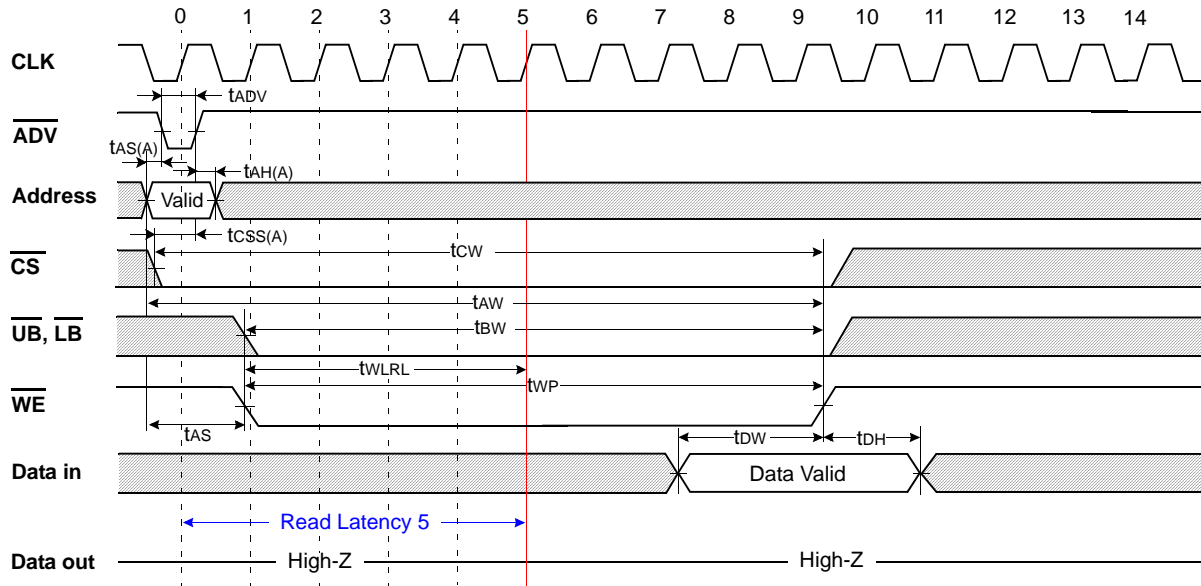
Table 22. ASYNCHRONOUS WRITE AC CHARACTERISTICS(\overline{UB} & \overline{LB} Controlled)

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
t_{WC}	70	-	ns	t_{AS}	0	-	ns
t_{CW}	60	-	ns	t_{WR}	0	-	ns
t_{AW}	60	-	ns	t_{DW}	30	-	ns
t_{BW}	60	-	ns	t_{DH}	0	-	ns
t_{WP}	55 ¹⁾	-	ns				

1. $t_{WP}(\text{min})=70\text{ns}$ for continuous write operation over 50 times.

ASYNCHRONOUS WRITE TIMING WAVEFORM in SYNCHRONOUS MODE

Fig.19 TIMING WAVEFORM OF WRITE CYCLE(Address Latch Type)($\overline{MRS}=V_{IH}$, $\overline{OE}=V_{IH}$, $\overline{WAIT}=High-Z$, \overline{WE} Controlled)



(ADDRESS LATCH TYPE ASYNCHRONOUS WRITE CYCLE - \overline{WE} Controlled)

1. A write occurs during the overlap(t_{WP}) of low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for word operation. A write ends at the earliest transition when \overline{CS} goes high or \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{AW} is measured from the address valid to the end of write. In this address latch type write timing, t_{WC} is same as t_{AW} .
3. t_{CW} is measured from the \overline{CS} going low to the end of write.
4. t_{BW} is measured from the \overline{UB} and \overline{LB} going low to the end of write.
5. Clock input does not have any affect to the write operation if the parameter t_{WLR} is met.

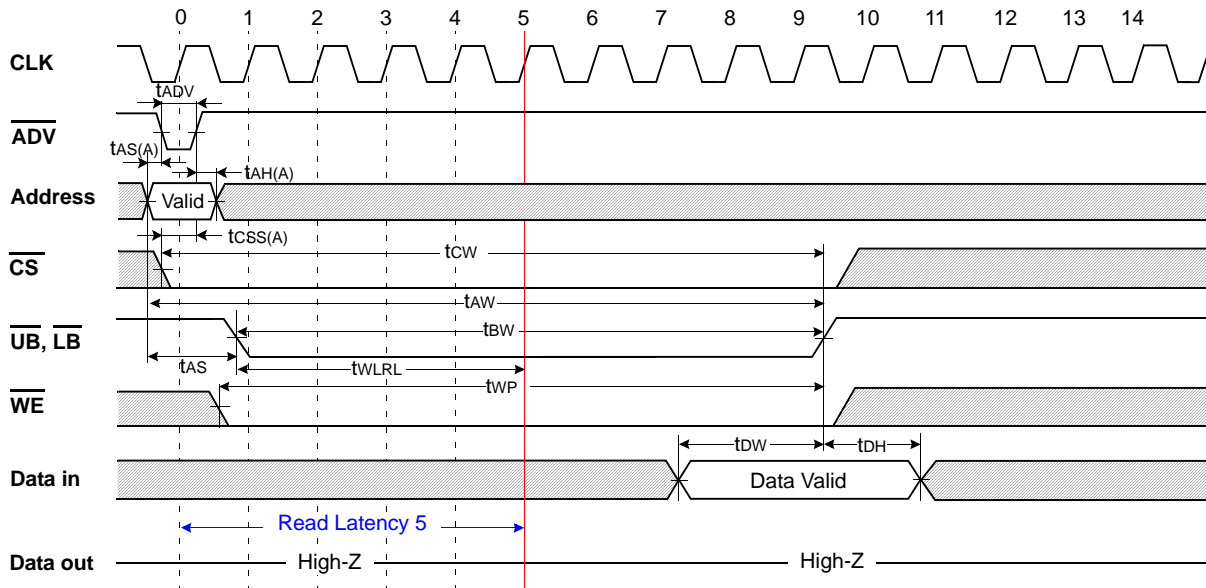
Table 23. ASYNCH. WRITE IN SYNCH. MODE AC CHARACTERISTICS(Address Latch Type, \overline{WE} Controlled)

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
t_{ADV}	7	-	ns	t_{BW}	60	-	ns
$t_{AS(A)}$	0	-	ns	t_{WP}	55 ¹⁾	-	ns
$t_{AH(A)}$	7	-	ns	t_{WLR}	1	-	clock
$t_{CSS(A)}$	10	-	ns	t_{AS}	0	-	ns
t_{CW}	60	-	ns	t_{DW}	30	-	ns
t_{AW}	60	-	ns	t_{DH}	0	-	ns

1. $t_{WP}(\min)=70\text{ns}$ for continuous write operation over 50 times.

ASYNCHRONOUS WRITE TIMING WAVEFORM in SYNCHRONOUS MODE

Fig.20 TIMING WAVEFORM OF WRITE CYCLE(Address Latch Type)($\overline{MRS}=V_{IH}$, $\overline{OE}=V_{IH}$, $\overline{WAIT}=High-Z$, \overline{UB} & \overline{LB} Controlled)



(ADDRESS LATCH TYPE ASYNCHRONOUS WRITE CYCLE - \overline{UB} & \overline{LB} Controlled)

1. A write occurs during the overlap(t_{WP}) of low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for word operation. A write ends at the earliest transition when \overline{CS} goes or and \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{AW} is measured from the address valid to the end of write. In this address latch type write timing, t_{WC} is same as t_{AW} .
3. t_{CW} is measured from the \overline{CS} going low to the end of write.
4. t_{BW} is measured from the \overline{UB} and \overline{LB} going low to the end of write.
5. Clock input does not have any affect to the write operation if the parameter t_{WLR} is met.

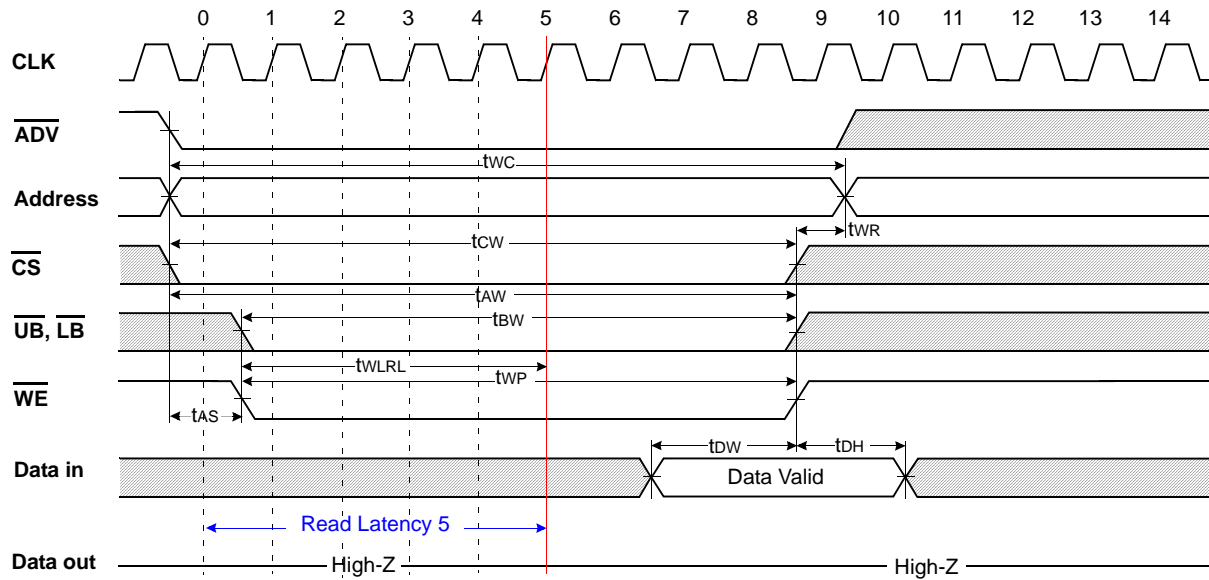
Table 24. ASYNCH. WRITE IN SYNCH. MODE AC CHARACTERISTICS(Address Latch Type, \overline{UB} & \overline{LB} Controlled)

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
t_{ADV}	7	-	ns	t_{BW}	60	-	ns
$t_{AS(A)}$	0	-	ns	t_{WP}	55 ¹⁾	-	ns
$t_{AH(A)}$	7	-	ns	t_{WLR}	1	-	clock
$t_{CSS(A)}$	10	-	ns	t_{AS}	0	-	ns
t_{CW}	60	-	ns	t_{DW}	30	-	ns
t_{AW}	60	-	ns	t_{DH}	0	-	ns

1. $t_{WP}(\min)=70\text{ns}$ for continuous write operation over 50 times.

ASYNCHRONOUS WRITE TIMING WAVEFORM in SYNCHRONOUS MODE

Fig.21 TIMING WAVEFORM OF WRITE CYCLE(Low \overline{ADV} Type)($\overline{MRS}=V_{IH}$, $\overline{OE}=V_{IH}$, $\overline{WAIT}=High-Z$, \overline{WE} Controlled)



(LOW \overline{ADV} TYPE WRITE CYCLE - \overline{WE} Controlled)

1. A write occurs during the overlap(t_{WP}) of low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when \overline{CS} goes high or \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS} going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with \overline{CS} or \overline{WE} going high.
5. Clock input does not have any affect to the write operation if the parameter t_{WLR} is met.

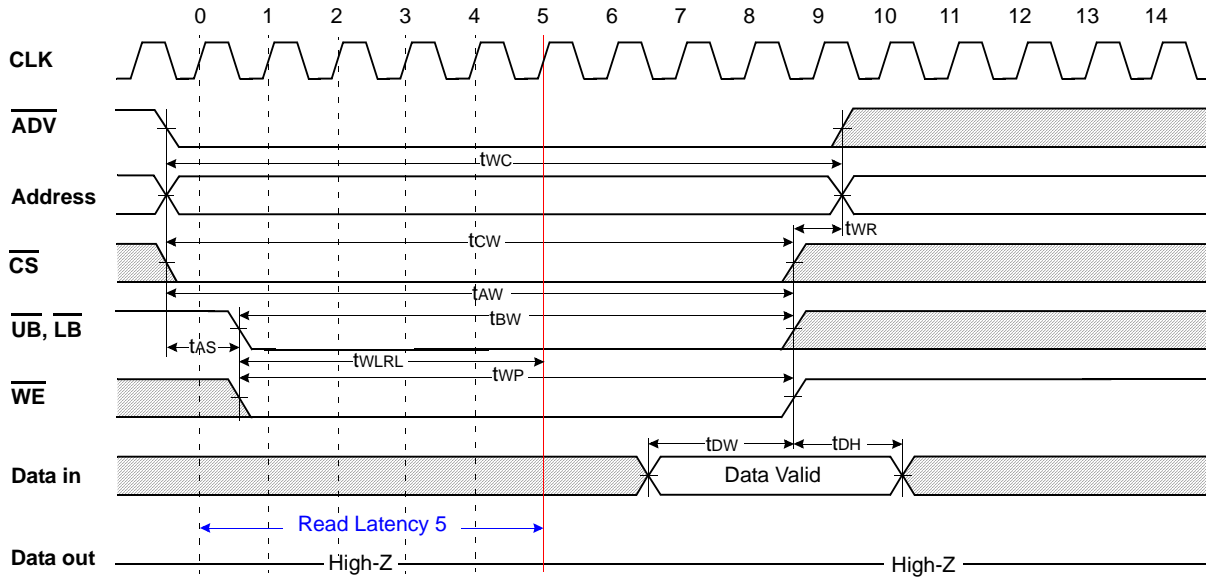
Table 25. ASYNCH. WRITE IN SYNCH. MODE AC CHARACTERISTICS(Low \overline{ADV} Type, \overline{WE} Controlled)

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
t_{WC}	70	-	ns	t_{WLR}	1	-	clock
t_{CW}	60	-	ns	t_{AS}	0	-	ns
t_{AW}	60	-	ns	t_{WR}	0	-	ns
t_{BW}	60	-	ns	t_{DW}	30	-	ns
t_{WP}	55 ¹⁾	-	ns	t_{DH}	0	-	ns

1. $t_{WP}(\text{min})=70\text{ns}$ for continuous write operation over 50 times.

ASYNCHRONOUS WRITE TIMING WAVEFORM in SYNCHRONOUS MODE

Fig.22 TIMING WAVEFORM OF WRITE CYCLE(Low ADV Type)($\overline{MRS}=V_{IH}$, $\overline{OE}=V_{IH}$, $\overline{WAIT}=High-Z$, \overline{UB} & \overline{LB} Controlled)



(LOW ADV TYPE WRITE CYCLE - \overline{UB} & \overline{LB} Controlled)

1. A write occurs during the overlap(t_{WP}) of low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when \overline{CS} goes high or \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS} going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with \overline{CS} or \overline{WE} going high.
5. Clock input does not have any affect to the write operation if the parameter t_{WLR} is met.

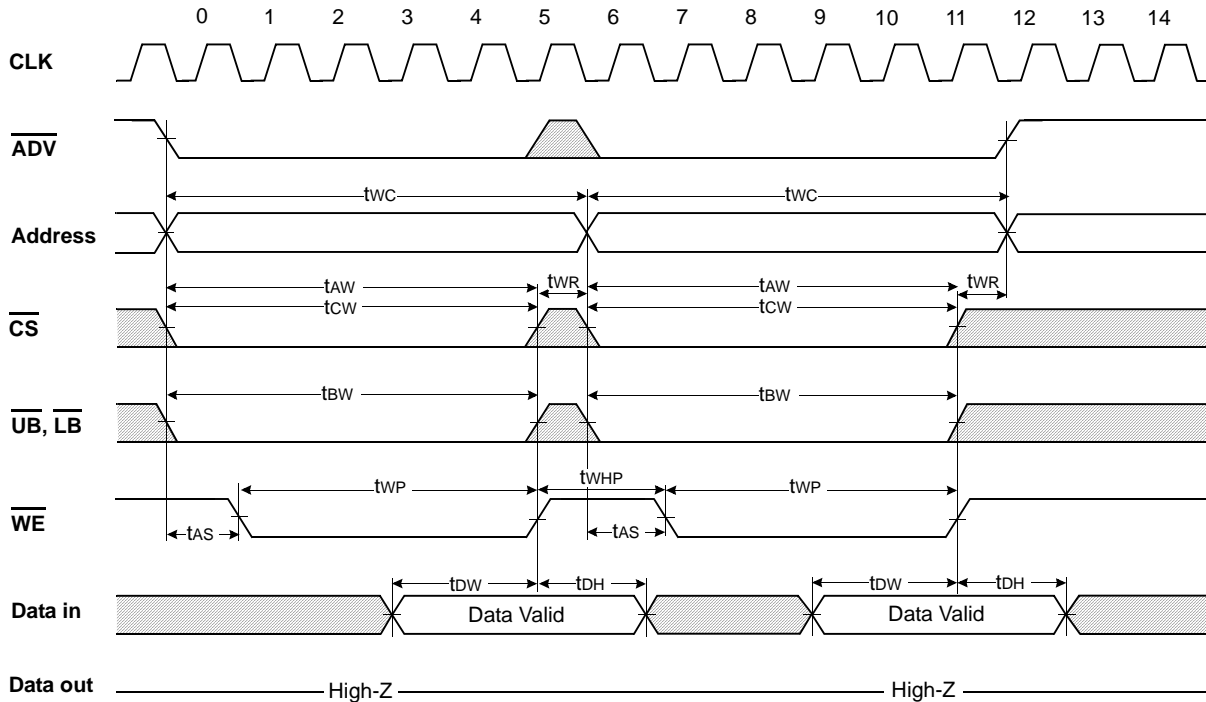
Table 26. ASYNCH. WRITE IN SYNCH. MODE AC CHARACTERISTICS(Low ADV Type, \overline{UB} & \overline{LB} Controlled)

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
t_{WC}	70	-	ns	t_{WLR}	1	-	clock
t_{CW}	60	-	ns	t_{AS}	0	-	ns
t_{AW}	60	-	ns	t_{WR}	0	-	ns
t_{BW}	60	-	ns	t_{DW}	30	-	ns
t_{WP}	55 ¹⁾	-	ns	t_{DH}	0	-	ns

1. $t_{WP}(\min)=70\text{ns}$ for continuous write operation over 50 times.

ASYNCHRONOUS WRITE TIMING WAVEFORM in SYNCHRONOUS MODE

Fig.23 TIMING WAVEFORM OF MULTIPLE WRITE CYCLE(Low \overline{ADV} Type)($\overline{MRS}=V_{IH}$, $\overline{OE}=V_{IH}$, $\overline{WAIT}=High-Z$, \overline{WE} Controlled)



(LOW \overline{ADV} TYPE MULTIPLE WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when \overline{CS} goes high or \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS} going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with \overline{CS} or \overline{WE} going high.
5. Clock input does not have any affect to the asynchronous multiple write operation if t_{WHP} is shorter than (Read Latency - 1) clock duration.
6. $t_{WP}(\min)=70\text{ns}$ for continuous write operation over 50 times.

Table 27. ASYNCH. WRITE IN SYNCH. MODE AC CHARACTERISTICS(Low \overline{ADV} Type Multiple Write, \overline{WE} Controlled)

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
t_{WC}	70	-	ns	t_{WHP}	5ns	Latency-1 clock	-
t_{CW}	60	-	ns	t_{AS}	0	-	ns
t_{AW}	60	-	ns	t_{WR}	0	-	ns
t_{BW}	60	-	ns	t_{DW}	30	-	ns
t_{WP}	55 ¹⁾	-	ns	t_{DH}	0	-	ns

1. $t_{WP}(\min)=70\text{ns}$ for continuous write operation over 50 times.

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Test Input/Output Reference)

Input pulse level: 0.2 to Vcc-0.2V
 Input rising and falling time: 3ns
 Input and output reference voltage: 0.5 x Vcc
 Output load: CL=30pF

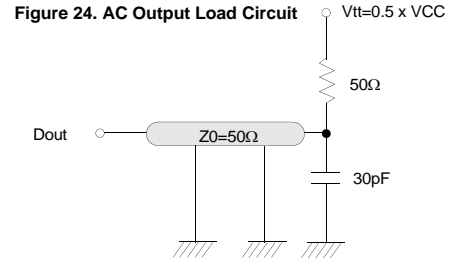


Table 28. SYNCHRONOUS AC CHARACTERISTICS (Vcc=1.7~2.0V, TA=-40 to 85°C, Maximum Main Clock Frequency=66MHz)

Parameter List	Symbol	Speed		Units	
		Min	Max		
Burst Operation (Common)	Clock Cycle Time	T	15	200	ns
	Burst Cycle Time	tBC	-	2500	ns
	Address Set-up Time to \overline{ADV} Falling(Burst)	tAS(B)	0	-	ns
	Address Hold Time from \overline{ADV} Rising(Burst)	tAH(B)	7	-	ns
	\overline{ADV} Setup Time	tADVS	5	-	ns
	\overline{ADV} Hold Time	tADVH	7	-	ns
	\overline{CS} Setup Time to Clock Rising(Burst)	tCSS(B)	5	-	ns
	Burst End to New \overline{ADV} Falling	tBEADV	7	-	ns
	Burst Stop to New \overline{ADV} Falling	tBSADV	12	-	ns
	\overline{CS} Low Hold Time from Clock	tCSLH	7	-	ns
	\overline{CS} High Pulse Width	tCSHP	5	-	ns
	\overline{ADV} High Pulse Width	tADHP	5	-	ns
	Chip Select to \overline{WAIT} Low	tWL	-	10	ns
	\overline{ADV} Falling to \overline{WAIT} Low	tAWL	-	10	ns
	Clock to \overline{WAIT} High	tWH	-	12	ns
Chip De-select to \overline{WAIT} High-Z	tWZ	-	12	ns	
Burst Read Operation	\overline{UB} , \overline{LB} Enable to End of Latency Clock	tBEL	1	-	Clock
	Output Enable to End of Latency Clock	toEL	1	-	Clock
	\overline{UB} , \overline{LB} Valid to Low-Z Output	tBLZ	5	-	ns
	Output Enable to Low-Z Output	toLZ	5	-	ns
	Latency Clock Rising Edge to Data Output	tCD	-	10	ns
	Output Hold	toH	3	-	ns
	Burst End Clock to Output High-Z	thZ	-	12	ns
	Chip De-select to Output High-Z	tCHZ	-	12	ns
	Output Disable to Output High-Z	toHZ	-	12	ns
	\overline{UB} , \overline{LB} Disable to Output High-Z	tBHZ	-	12	ns
Burst Write Operation	\overline{WE} Set-up Time to Command Clock	twES	5	-	ns
	\overline{WE} Hold Time from Command Clock	tWEH	5	-	ns
	\overline{WE} High Pulse Width	twHP	5	-	ns
	\overline{UB} , \overline{LB} Set-up Time to Clock	tBS	5	-	ns
	\overline{UB} , \overline{LB} Hold Time from Clock	tBH	5	-	ns
	Byte Masking Set-up Time to Clock	tBMS	7	-	ns
	Byte Masking Hold Time from Clock	tBMH	7	-	ns
	Data Set-up Time to Clock	tDS	5	-	ns
Data Hold Time from Clock	tdHC	3	-	ns	

SYNCHRONOUS BURST OPERATION TIMING WAVEFORM

Fig.25 TIMING WAVEFORM OF BASIC BURST OPERATION [Latency=5, Burst Length=4]($\overline{MRS}=V_{IH}$)

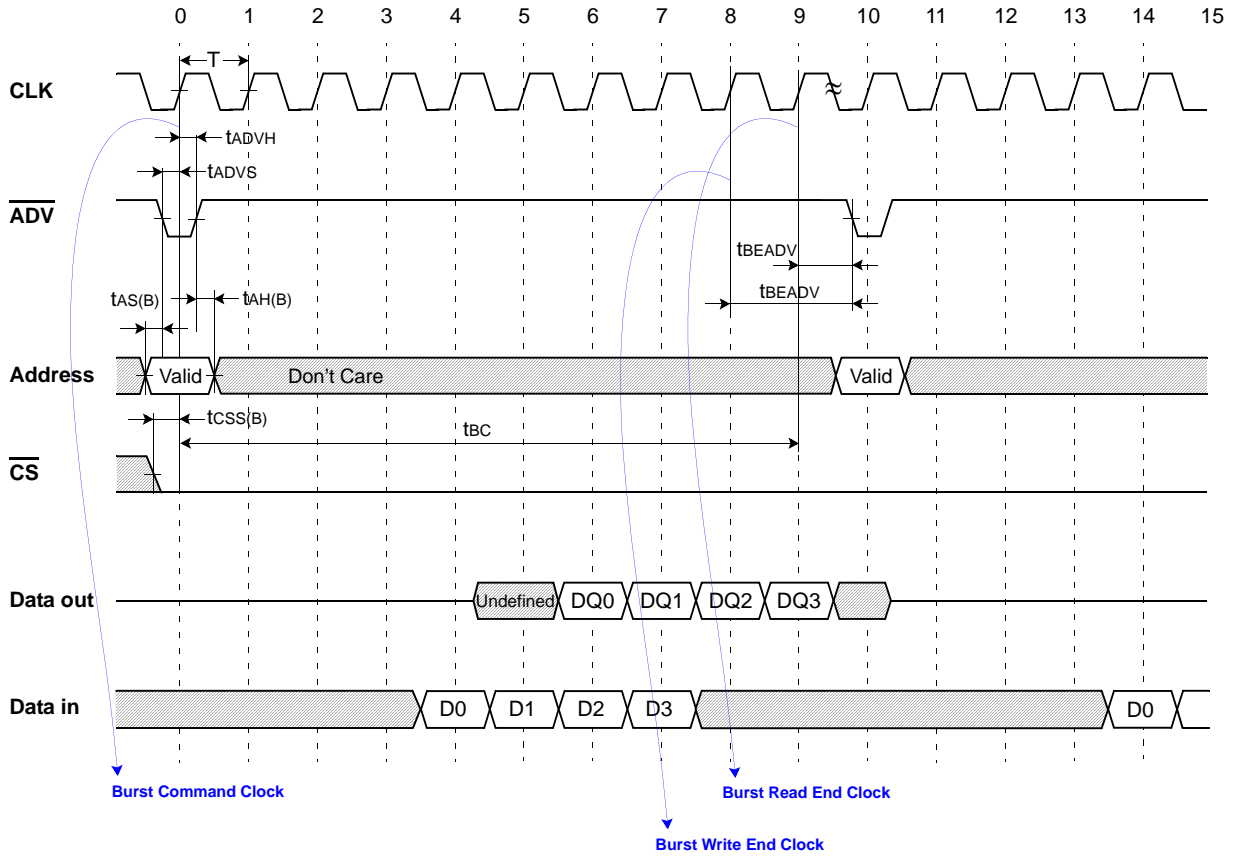
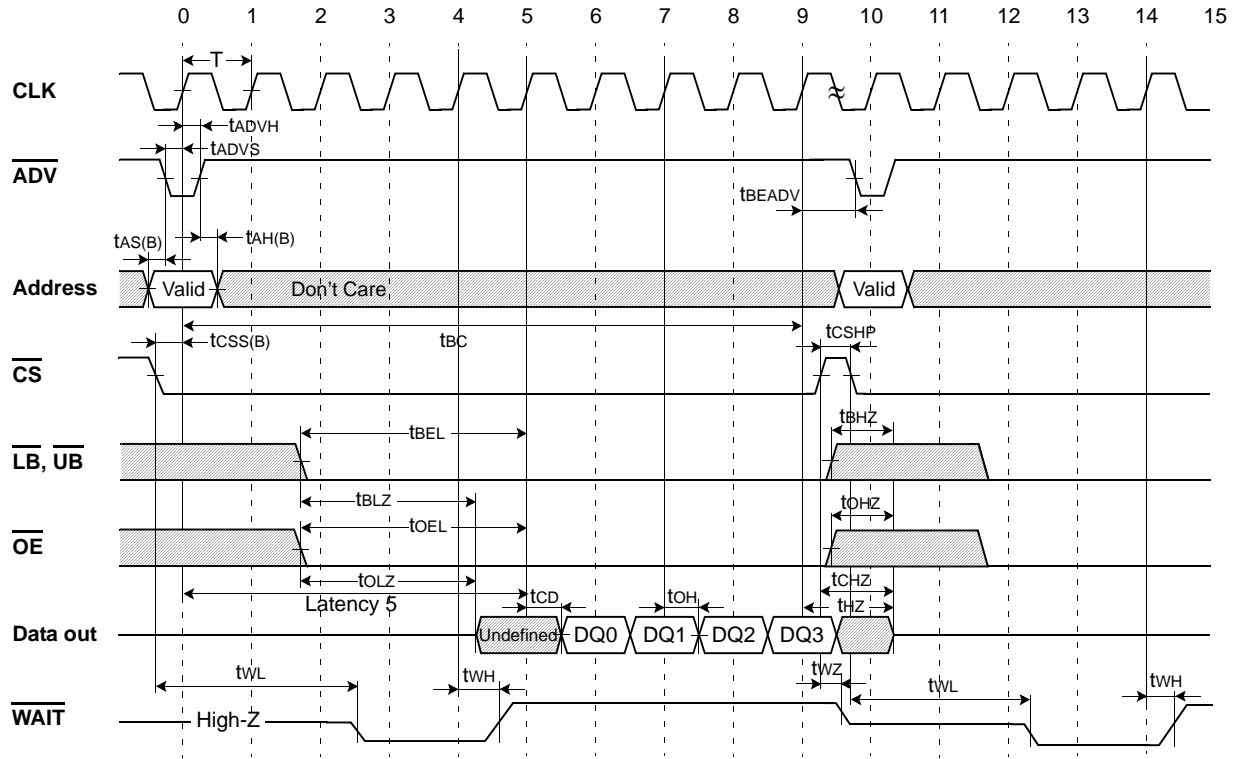


Table 29. BURST OPERATION AC CHARACTERISTICS

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
T	15	200	ns	tAS(B)	0	-	ns
tBC	-	2500	ns	tAH(B)	7	-	ns
tADVS	5	-	ns	tCSS(B)	5	-	ns
tADVH	7	-	ns	tBEADV	7	-	ns

SYNCHRONOUS BURST READ TIMING WAVEFORM

Fig.26 TIMING WAVEFORM OF BURST READ CYCLE(1) [Latency=5, Burst Length=4, WP=Low enable]($\overline{WE}=V_{IH}$, $\overline{MRS}=V_{IH}$) - CS Toggling Consecutive Burst Read



(SYNCHRONOUS BURST READ CYCLE - \overline{CS} Toggling Consecutive Burst Read)

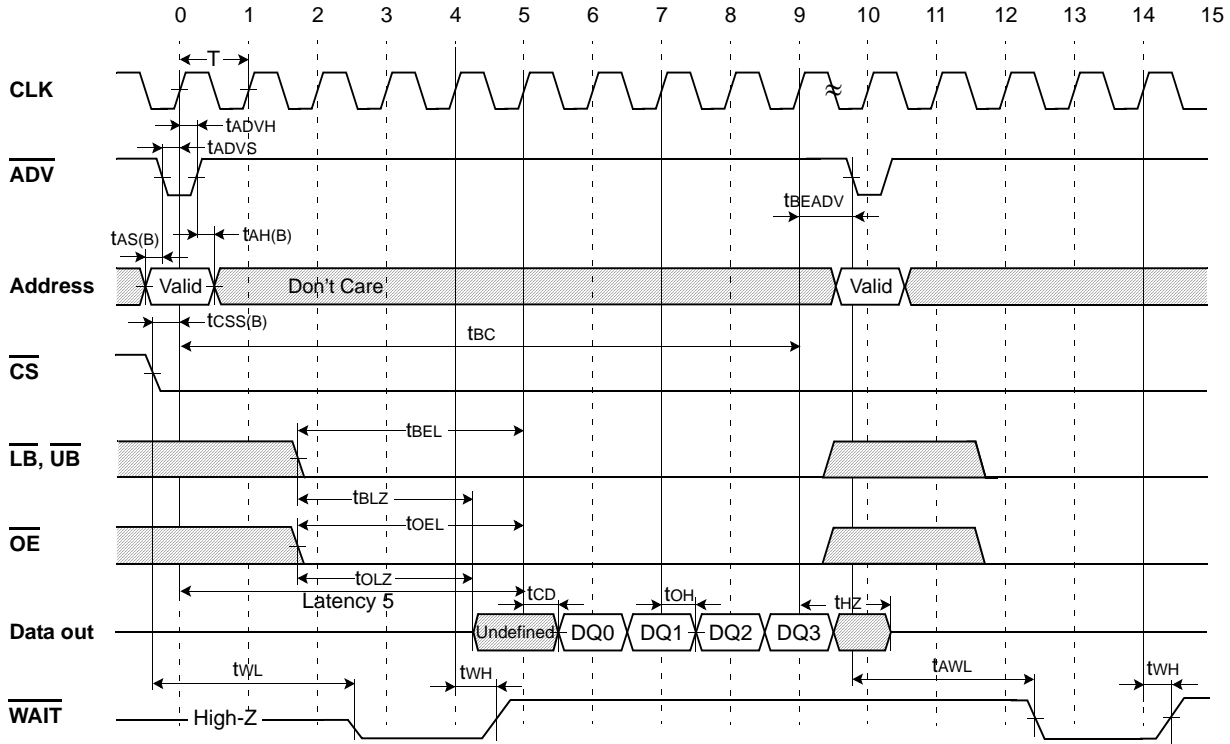
1. The new burst operation can be issued only after the previous burst operation is finished. For the new burst operation, tBEADV should be met.
2. /WAIT Low(tWL or tAWL) : Data not available(driven by \overline{CS} low going edge or \overline{ADV} low going edge)
 /WAIT High(tWH) : Data available(driven by Latency-1 clock)
 /WAIT High-Z(tWZ) : Data don't care(driven by \overline{CS} high going edge)
3. Multiple clock risings are allowed during low \overline{ADV} period. The burst operation starts from the first clock rising.
4. Burst Cycle Time(tBC) should not be over 2.5 μ s.

Table 30. BURST READ AC CHARACTERISTICS(\overline{CS} Toggling Consecutive Burst)

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tCSHP	5	-	ns	tOHZ	-	12	ns
tBEL	1	-	clock	tBHZ	-	12	ns
tOEL	1	-	clock	tCD	-	10	ns
tBLZ	5	-	ns	tOH	3	-	ns
tOLZ	5	-	ns	tWL	-	10	ns
tHZ	-	12	ns	tWH	-	12	ns
tCHZ	-	12	ns	tWZ	-	12	ns

SYNCHRONOUS BURST READ TIMING WAVEFORM

Fig.27 TIMING WAVEFORM OF BURST READ CYCLE(2) [Latency=5, Burst Length=4, WP=Low enable]($\overline{WE}=V_{IH}$, $\overline{MRS}=V_{IH}$)
- CS Low Holding Consecutive Burst Read



(SYNCHRONOUS BURST READ CYCLE - \overline{CS} Low Holding Consecutive Burst Read)

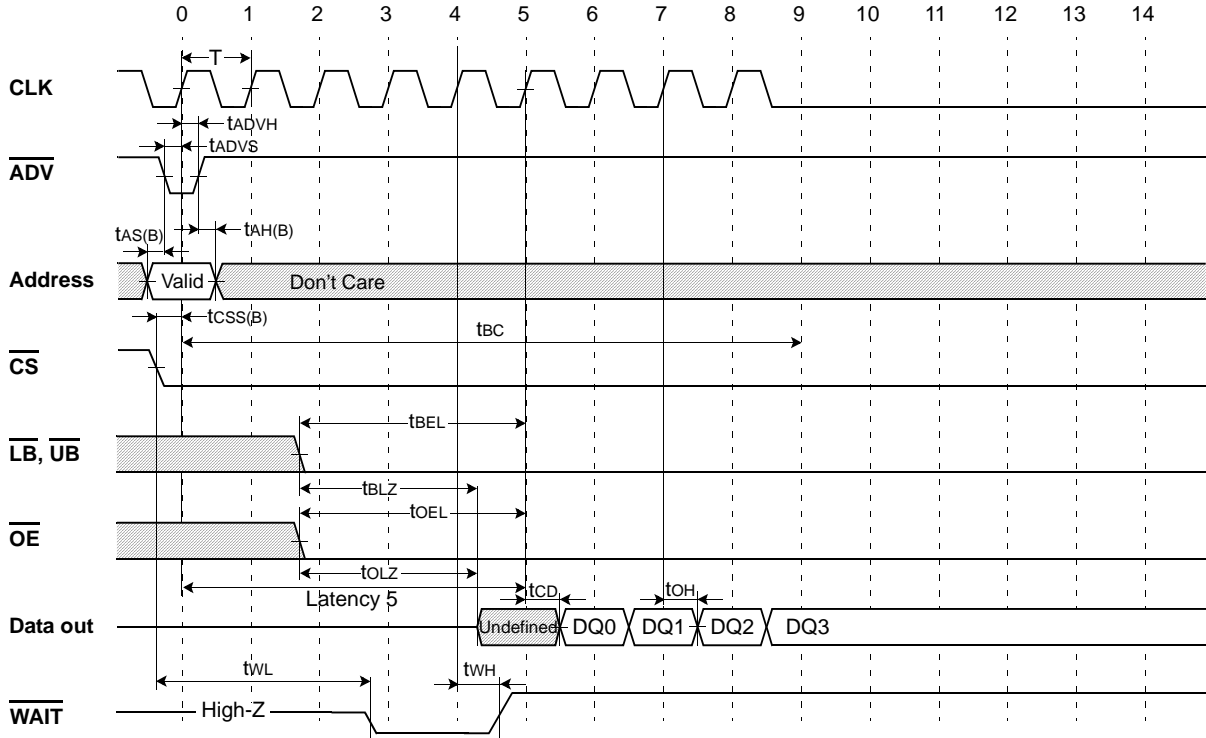
- The new burst operation can be issued only after the previous burst operation is finished. For the new burst operation, tBEADV should be met.
- /WAIT Low (tWL or tAWL) : Data not available (driven by \overline{CS} low going edge or \overline{ADV} low going edge)
/WAIT High (tWH) : Data available (driven by Latency-1 clock)
/WAIT High-Z (tWZ) : Data don't care (driven by \overline{CS} high going edge)
- Multiple clock risings are allowed during low \overline{ADV} period. The burst operation starts from the first clock rising.
- The consecutive multiple burst read operation with holding \overline{CS} low is possible through issuing only new \overline{ADV} and address.
- Burst Cycle Time (tBC) should not be over 2.5 μ s.

Table 31. BURST READ AC CHARACTERISTICS (\overline{CS} Low Holding Consecutive Burst)

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tBEL	1	-	clock	tCD	-	10	ns
tOEL	1	-	clock	tOH	3	-	ns
tBLZ	5	-	ns	tWL	-	10	ns
tOLZ	5	-	ns	tAWL	-	10	ns
tHZ	-	12	ns	tWH	-	12	ns

SYNCHRONOUS BURST READ TIMING WAVEFORM

Fig.28 TIMING WAVEFORM OF BURST READ CYCLE(3) [Latency=5, Burst Length=4, WP=Low enable]($\overline{WE}=V_{IH}$, $\overline{MRS}=V_{IH}$)
 - Last Data Sustaining



(SYNCHRONOUS BURST READ CYCLE - Last Data Sustaining)

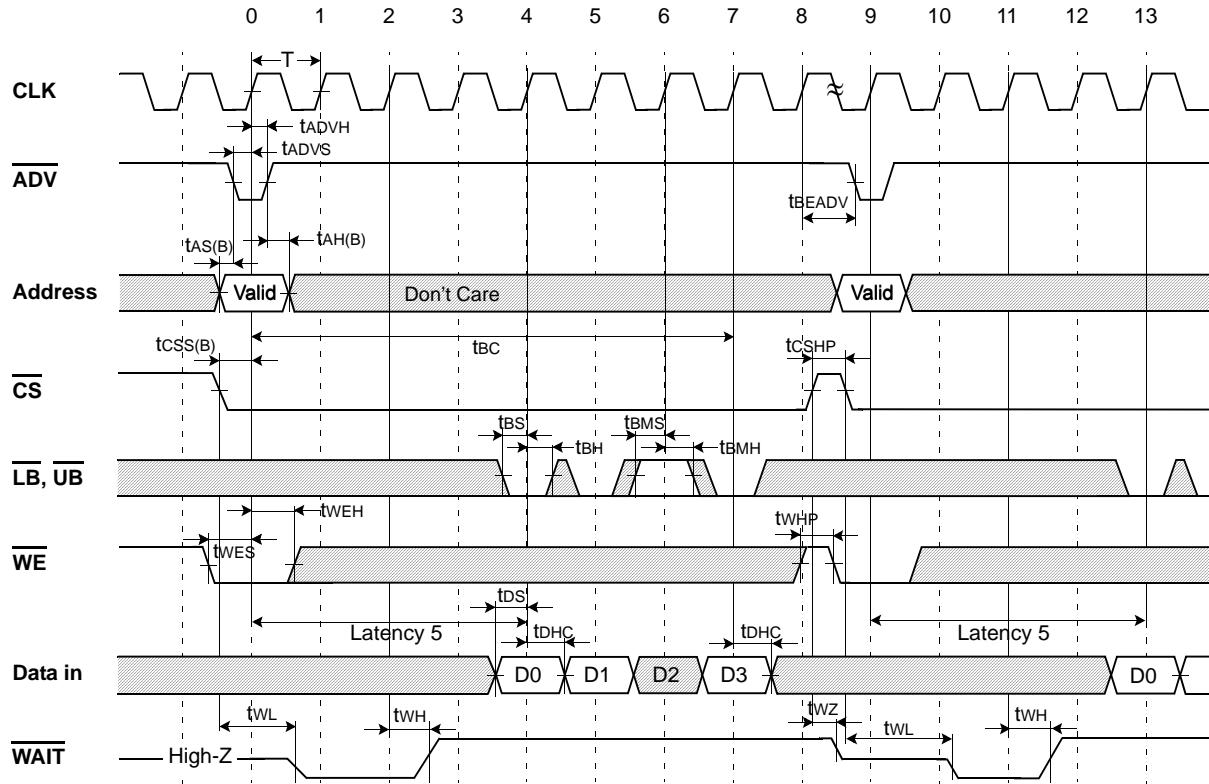
1. /WAIT Low(tWL or tAWL) : Data not available(driven by CS low going edge or ADV low going edge)
 /WAIT High(tWH) : Data available(driven by Latency-1 clock)
 /WAIT High-Z(tWZ) : Data don't care(driven by CS high going edge)
2. Multiple clock risings are allowed during low ADV period. The burst operation starts from the first clock rising.
3. Burst Cycle Time(tBC) should not be over 2.5μs.

Table 32. BURST READ AC CHARACTERISTICS (Last Data Sustaining)

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tBEL	1	-	clock	tCD	-	10	ns
tOEL	1	-	clock	tOH	3	-	ns
tBLZ	5	-	ns	tWL	-	10	ns
tOLZ	5	-	ns	tWH	-	12	ns

SYNCHRONOUS BURST WRITE TIMING WAVEFORM

Fig.29 TIMING WAVEFORM OF BURST WRITE CYCLE(1) [Latency=5, Burst Length=4, WP=Low enable] ($\overline{OE}=V_{IH}$, $\overline{MRS}=V_{IH}$) - CS Toggling Consecutive Burst Write



(SYNCHRONOUS BURST WRITE CYCLE - \overline{CS} Toggling Consecutive Burst Write)

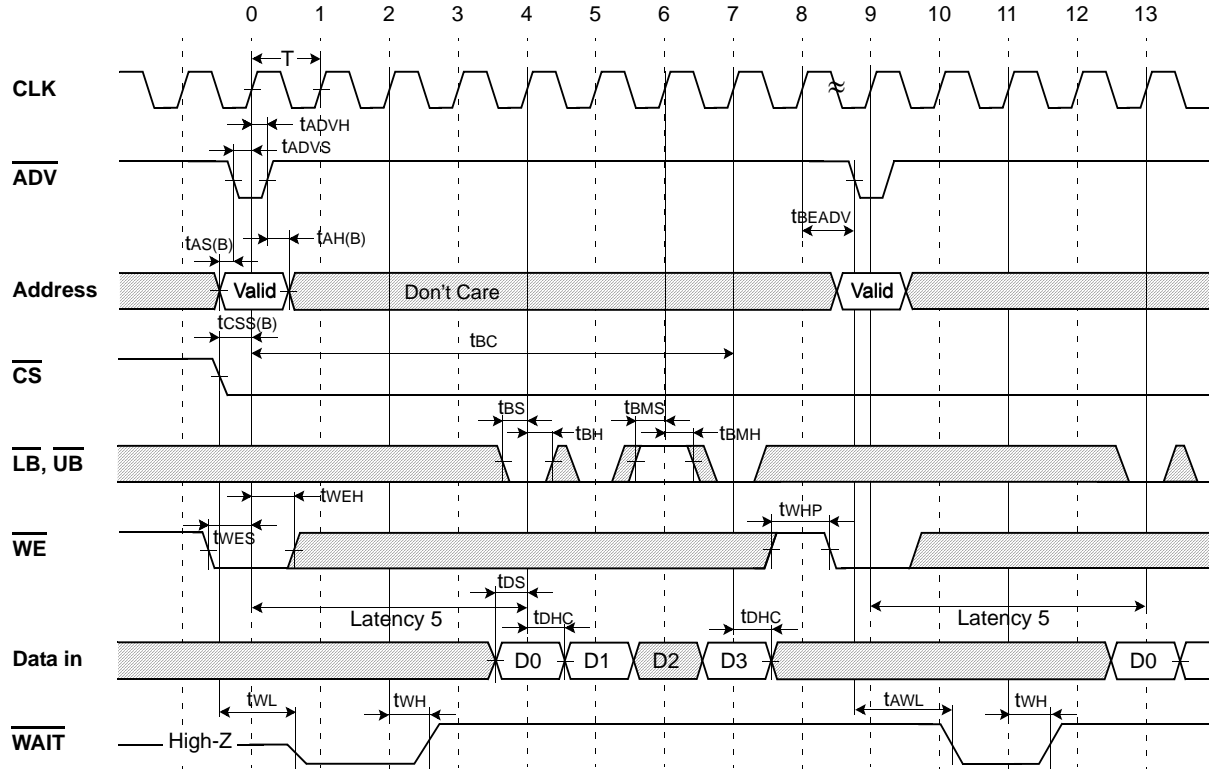
1. The new burst operation can be issued only after the previous burst operation is finished. For the new burst operation, t_{BEADV} should be met.
2. Multiple clock risings are allowed during low \overline{ADV} period. The burst operation starts from the first clock rising.
3. \overline{WAIT} Low (t_{WL} or t_{AWL}) : Data not available (driven by \overline{CS} low going edge or \overline{ADV} low going edge)
 \overline{WAIT} High (t_{WH}) : Data available (driven by Latency-1 clock)
 \overline{WAIT} High-Z (t_{WZ}) : Data don't care (driven by \overline{CS} high going edge)
4. D2 is masked by UB and LB.
5. Burst Cycle Time (t_{BC}) should not be over 2.5 μ s.

Table 33. BURST WRITE AC CHARACTERISTICS (\overline{CS} Toggling Consecutive Burst)

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
t_{CSHP}	5	-	ns	t_{WHP}	5	-	ns
t_{BS}	5	-	ns	t_{DS}	5	-	ns
t_{BH}	5	-	ns	t_{DHC}	3	-	ns
t_{BMS}	7	-	ns	t_{WL}	-	10	ns
t_{BMH}	7	-	ns	t_{WH}	-	12	ns
t_{WES}	5	-	ns	t_{WZ}	-	12	ns
t_{WEH}	5	-	ns				

SYNCHRONOUS BURST WRITE TIMING WAVEFORM

Fig.30 TIMING WAVEFORM OF BURST WRITE CYCLE(2) [Latency=5,Burst Length=4,WP=Low enable]($\overline{OE}=V_{IH}$, $\overline{MRS}=V_{IH}$) - CS Low Holding Consecutive Burst Write



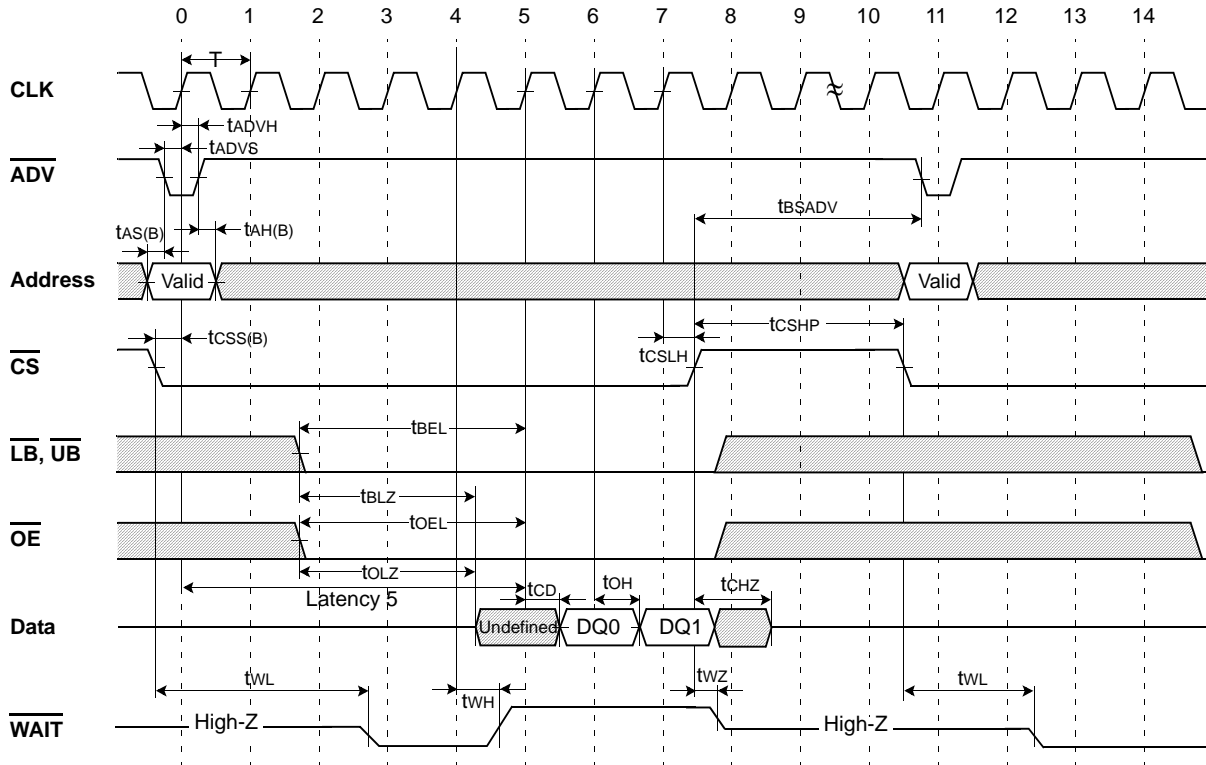
- (SYNCHRONOUS BURST WRITE CYCLE - \overline{CS} Low Holding Consecutive Burst Write)
1. The new burst operation can be issued only after the previous burst operation is finished. For the new burst operation, t_{BEADV} should be met.
 2. Multiple clock risings are allowed during low \overline{ADV} period. The burst operation starts from the first clock rising.
 3. \overline{WAIT} Low (t_{WL} or t_{AWL}) : Data not available (driven by \overline{CS} low going edge or \overline{ADV} low going edge)
 \overline{WAIT} High (t_{WH}) : Data available (driven by Latency-1 clock)
 \overline{WAIT} High-Z (t_{WZ}) : Data don't care (driven by \overline{CS} high going edge)
 4. D2 is masked by \overline{UB} and \overline{LB} .
 5. The consecutive multiple burst read operation with holding \overline{CS} low is possible through issuing only new \overline{ADV} and address.
 6. Burst Cycle Time (t_{BC}) should not be over 2.5 μ s.

Table 34. BURST WRITE AC CHARACTERISTICS (\overline{CS} Low Holding Consecutive Burst)

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
t_{BS}	5	-	ns	t_{WHP}	5	-	ns
t_{BH}	5	-	ns	t_{DS}	5	-	ns
t_{BMS}	7	-	ns	t_{DHC}	3	-	ns
t_{BMH}	7	-	ns	t_{WL}	-	10	ns
t_{WES}	5	-	ns	t_{AWL}	-	10	ns
t_{WEH}	5	-	ns	t_{WH}	-	12	ns

SYNCHRONOUS BURST READ STOP TIMING WAVEFORM

Fig.31 TIMING WAVEFORM OF BURST READ STOP by \overline{CS} [Latency=5, Burst Length=4, WP=Low enable]($\overline{WE}=V_{IH}$, $\overline{MRS}=V_{IH}$)



(SYNCHRONOUS BURST READ STOP TIMING)

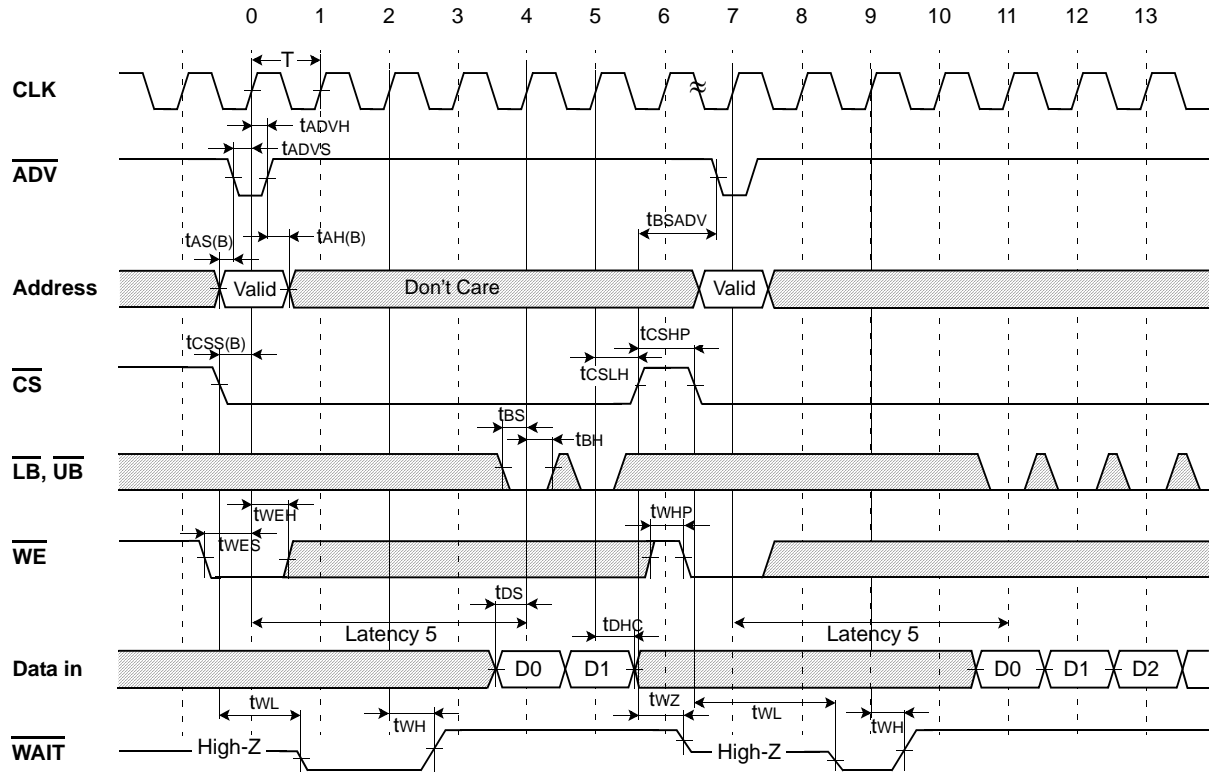
1. The new burst operation can be issued only after the previous burst operation is finished. For the new burst operation, tBSADV should be met
2. /WAIT Low(tWL or tAWL) : Data not available(driven by \overline{CS} low going edge or \overline{ADV} low going edge)
 /WAIT High(tWH) : Data available(driven by Latency-1 clock)
 /WAIT High-Z(tWZ) : Data don't care(driven by \overline{CS} high going edge)
3. Multiple clock risings are allowed during low ADV period. The burst operation starts from the first clock rising.
4. The burst stop operation should not be repeated for over 2.5 μ s.

Table 35. BURST READ STOP AC CHARACTERISTICS

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tBSADV	12	-	ns	tCD	-	10	ns
tCSSLH	7	-	ns	tOH	3	-	ns
tCSHP	5	-	ns	tCHZ	-	12	ns
tBEL	1	-	clock	tWL	-	10	ns
tOEL	1	-	clock	tWH	-	12	ns
tBLZ	5	-	ns	tWZ	-	12	ns
tOLZ	5	-	ns				

SYNCHRONOUS BURST WRITE STOP TIMING WAVEFORM

Fig.32 TIMING WAVEFORM OF BURST WRITE STOP by \overline{CS} [Latency=5, Burst Length=4, WP=Low enable]($\overline{OE}=V_{IH}$, $\overline{MRS}=V_{IH}$)



(SYNCHRONOUS BURST WRITE STOP TIMING)

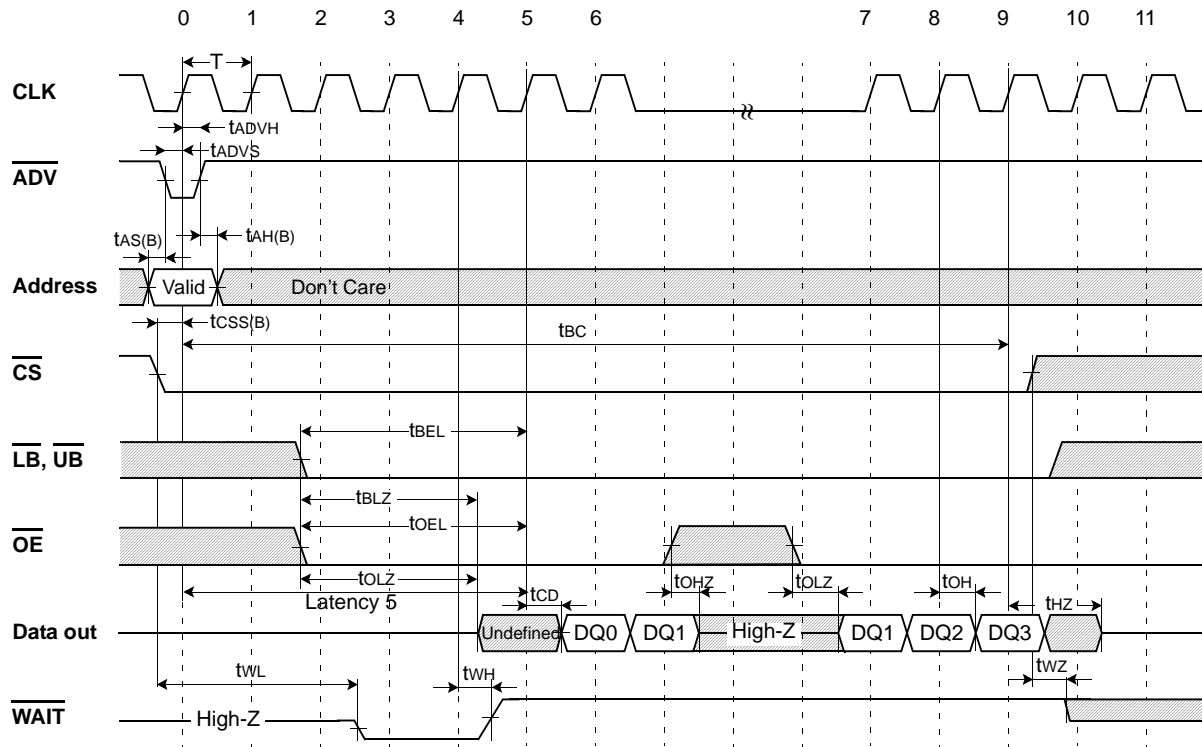
1. The new burst operation can be issued only after the previous burst operation is finished.
2. /WAIT Low(t_{WL} or t_{AWL}) : Data not available(driven by \overline{CS} low going edge or \overline{ADV} low going edge)
 /WAIT High(t_{WH}) : Data available(driven by Latency-1 clock)
 /WAIT High-Z(t_{WZ}) : Data don't care(driven by \overline{CS} high going edge)
3. Multiple clock risings are allowed during low \overline{ADV} period. The burst operation starts from the first clock rising.
4. The burst stop operation should not be repeated for over 2.5 μ s.

Table 36. BURST WRITE STOP AC CHARACTERISTICS

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tBSADV	12	-	ns	tWHP	5	-	ns
tCSLH	7	-	ns	tDS	5	-	ns
tCSHP	5	-	ns	tDQC	3	-	ns
tBS	5	-	ns	tWL	-	10	ns
tBH	5	-	ns	tWH	-	12	ns
tWES	5	-	ns	tWZ	-	12	ns
tWEH	5	-	ns				

SYNCHRONOUS BURST READ SUSPEND TIMING WAVEFORM

Fig.33 TIMING WAVEFORM OF BURST READ SUSPEND CYCLE(1) [Latency=5, Burst Length=4, WP=Low enable] ($\overline{WE}=V_{IH}$, $\overline{MRS}=V_{IH}$)



(SYNCHRONOUS BURST READ SUSPEND CYCLE)

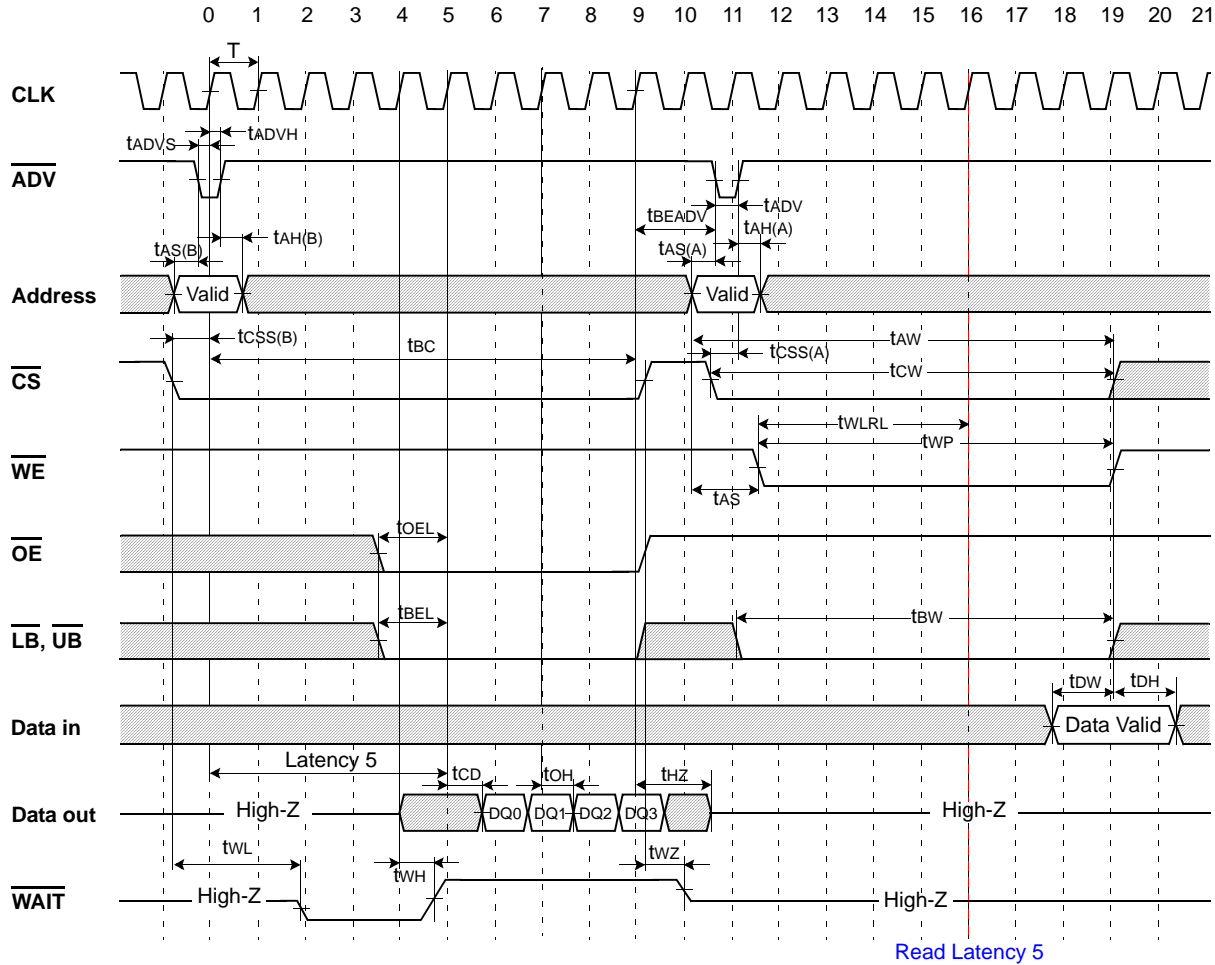
1. If clock input is halted during burst read operation, the data out will be suspended. During the burst read suspend period, \overline{OE} high drives data out to high-Z. If clock input is resumed, the suspended data will be out first.
2. /WAIT Low(t_{WL} or t_{AWL}) : Data not available(driven by \overline{CS} low going edge or \overline{ADV} low going edge)
 /WAIT High(t_{WH}) : Data available(driven by Latency-1 clock)
 /WAIT High-Z(t_{WZ}) : Data don't care(driven by \overline{CS} high going edge)
3. During suspend period, \overline{OE} high drives DQ to High-Z and \overline{OE} low drives DQ to Low-Z.
 If OE stays low during suspend period, the previous data will be sustained.
4. Burst Cycle Time(t_{BC}) should not be over 2.5 μ s.

Table 37. BURST READ SUSPEND AC CHARACTERISTICS

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
t_{BEL}	1	-	clock	t_{HZ}	-	12	ns
t_{OEL}	1	-	clock	t_{OHZ}	-	12	ns
t_{BLZ}	5	-	ns	t_{WL}	-	10	ns
t_{OLZ}	5	-	ns	t_{WH}	-	12	ns
t_{CD}	-	10	ns	t_{WZ}	-	12	ns
t_{OH}	3	-	ns				

TRANSITION TIMING WAVEFORM BETWEEN READ AND WRITE

Fig.34 SYNCH. BURST READ to ASYNCH. WRITE(Address Latch Type) TIMING WAVEFORM [Latency=5, Burst Length=4](MRS=V_H)



(SYNCHRONOUS BURST READ CYCLE)

1. The new burst operation can be issued only after the previous burst operation is finished. For the new burst operation, tBEADV should be met.
2. /WAIT Low(tWL or tAWL) : Data not available(driven by CS low going edge or ADV low going edge)
 /WAIT High(tWH) : Data available(driven by Latency-1 clock)
 /WAIT High-Z(tWZ) : Data don't care(driven by CS high going edge)
3. Multiple clock risings are allowed during low ADV period. The burst operation starts from the first clock rising.
4. Burst Cycle Time(tBC) should not be over 2.5μs.

(ADDRESS LATCH TYPE ASYNCHRONOUS WRITE CYCLE - WE controlled)

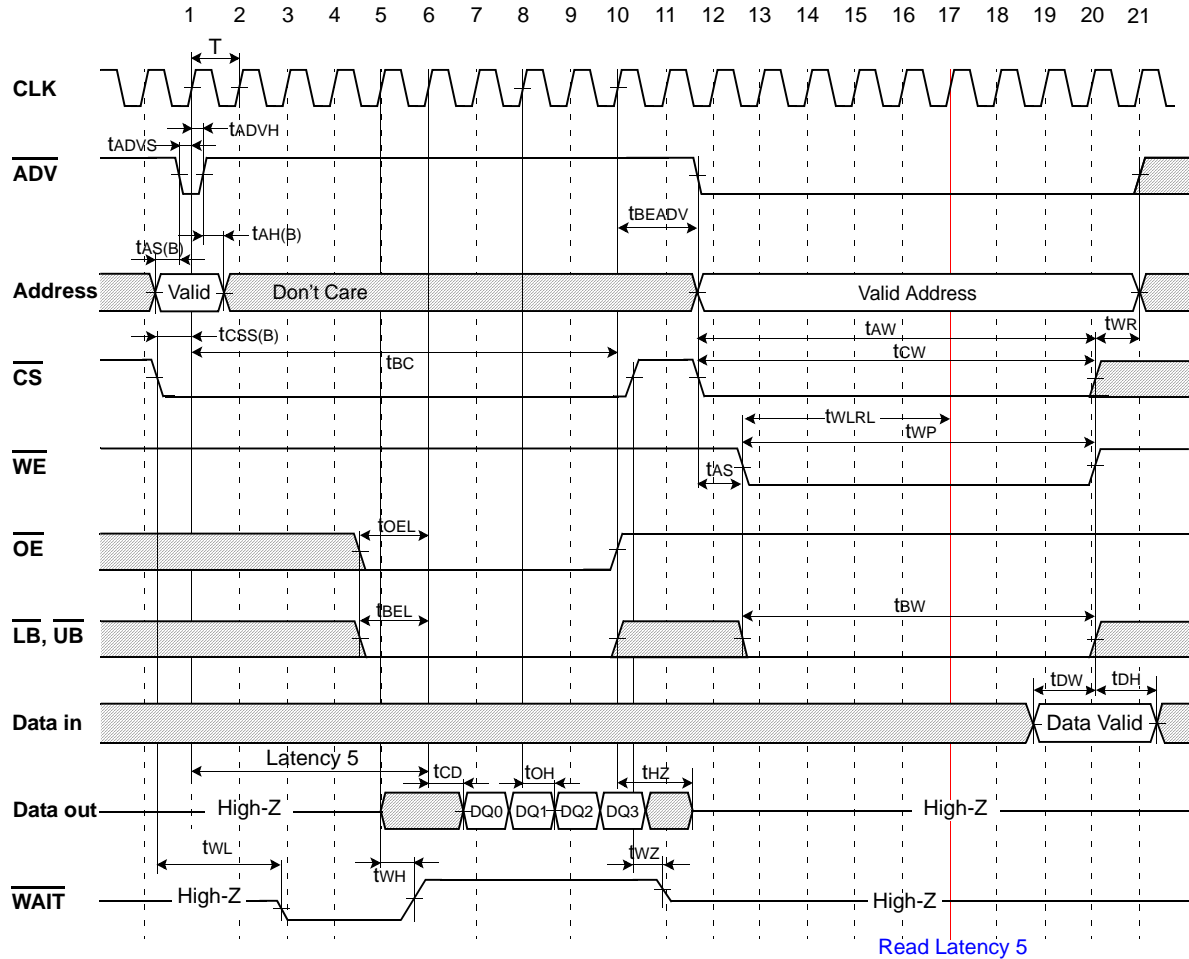
1. Clock input does not have any affect to the write operation if WE is driven to low before Read Latency-1 clock. Read Latency-1 clock in write timing is just a reference to WE low going for proper write operation.

Table 38. BURST READ to ASYNCH. WRITE(Address Latch Type) AC CHARACTERISTICS

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tBEADV	7	-	ns	tWLR	1	-	clock

TRANSITION TIMING WAVEFORM BETWEEN READ AND WRITE

Fig.35 SYNCH. BURST READ to ASYNCH. WRITE(Low ADV Type) TIMING WAVEFORM
 [Latency=5, Burst Length=4](MRS=V_H)



(SYNCHRONOUS BURST READ CYCLE)

1. The new burst operation can be issued only after the previous burst operation is finished. For the new burst operation, tBEADV should be met.
2. /WAIT Low(tWL or tAWL) : Data not available(driven by CS low going edge or ADV low going edge)
 /WAIT High(tWH) : Data available(driven by Latency-1 clock)
 /WAIT High-Z(tWZ) : Data don't care(driven by CS high going edge)
3. Multiple clock risings are allowed during low ADV period. The burst operation starts from the first clock rising.
4. Burst Cycle Time(tBC) should not be over 2.5μs.

(LOW ADV TYPE ASYNCHRONOUS WRITE CYCLE - WE controlled)

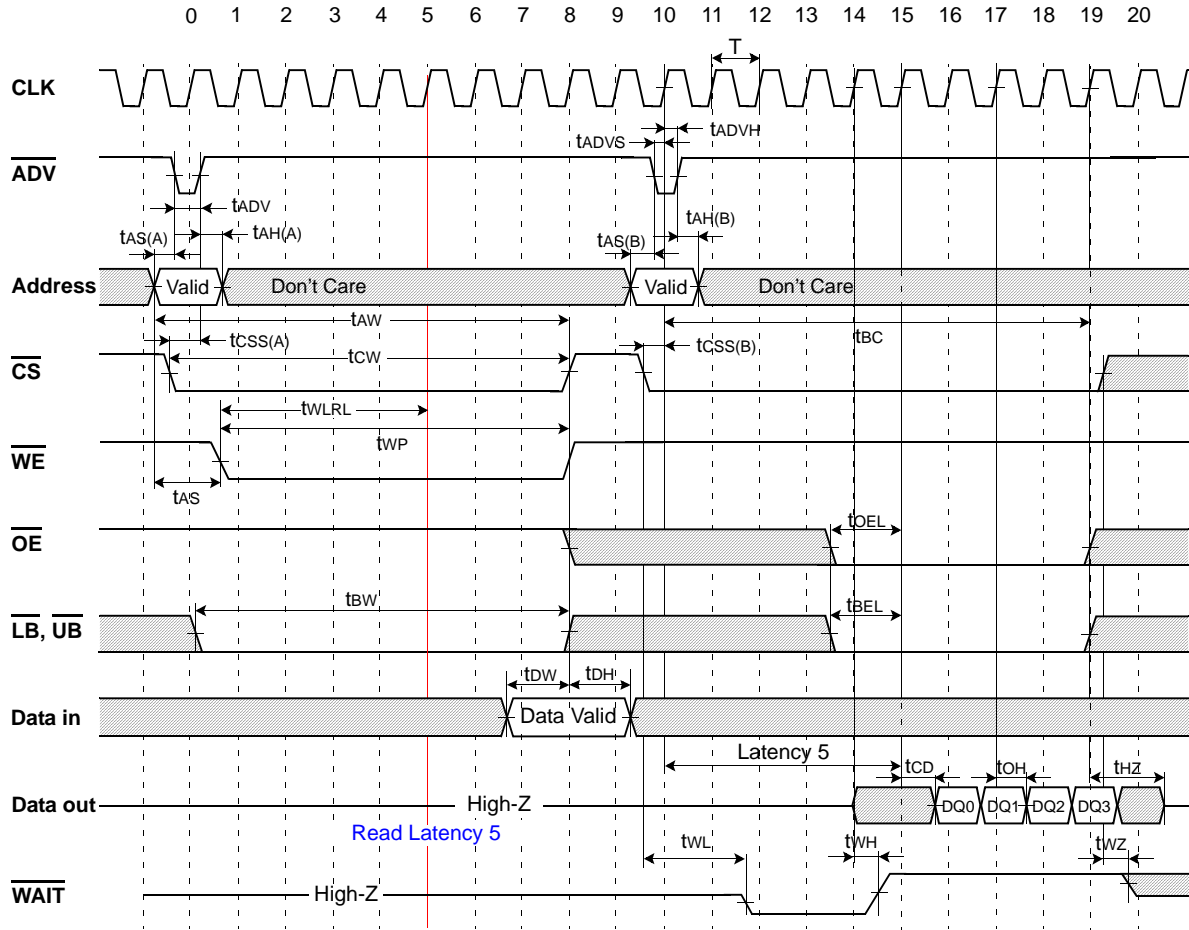
1. Clock input does not have any affect to the write operation if WE is driven to low before Read Latency-1 clock. Read Latency-1 clock in write timing is just a reference to WE low going for proper write operation.

Table 39. BURST READ to ASYNCH. WRITE(Low ADV Type) AC CHARACTERISTICS

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tBEADV	7	-	ns	tWLR	1	-	clock

TRANSITION TIMING WAVEFORM BETWEEN READ AND WRITE

Fig.36 ASYNCH. WRITE(Address Latch Type) to SYNCH. BURST READ TIMING WAVEFORM [Latency=5, Burst Length=4]($\overline{MRS}=V_{IH}$)



(SYNCHRONOUS BURST READ CYCLE)

1. The new burst operation can be issued only after the previous burst operation is finished. For the new burst operation, tBEADV should be met.
2. \overline{WAIT} Low (tWL or tAWL) : Data not available (driven by \overline{CS} low going edge or \overline{ADV} low going edge)
 \overline{WAIT} High (tWH) : Data available (driven by Latency-1 clock)
 \overline{WAIT} High-Z (tWZ) : Data don't care (driven by \overline{CS} high going edge)
3. Multiple clock risings are allowed during low \overline{ADV} period. The burst operation starts from the first clock rising.
4. Burst Cycle Time (tBC) should not be over 2.5 μ s.

(ADDRESS LATCH TYPE ASYNCHRONOUS WRITE CYCLE - \overline{WE} controlled)

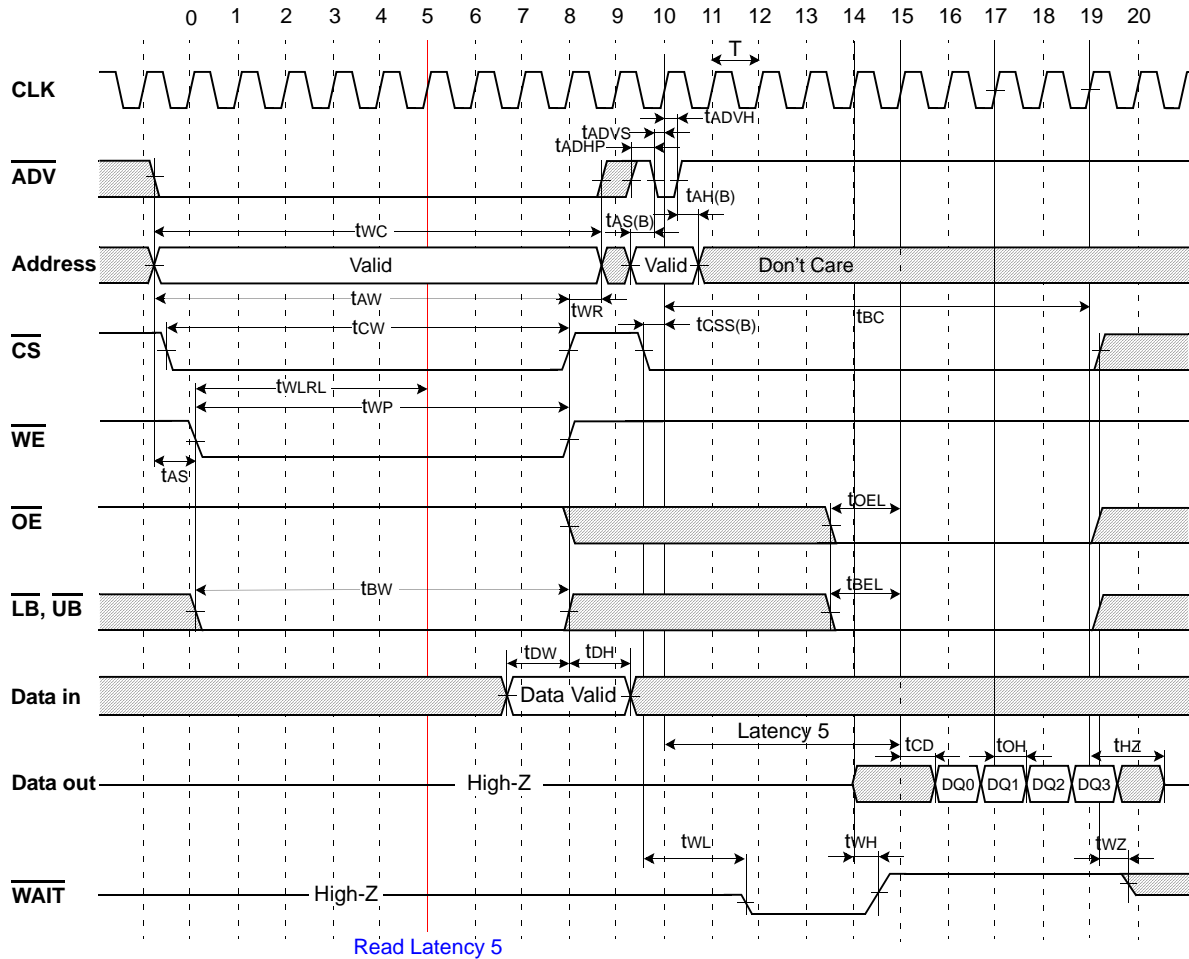
1. Clock input does not have any affect to the write operation if \overline{WE} is driven to low before Read Latency-1 clock. Read Latency-1 clock in write timing is just a reference to \overline{WE} low going for proper write operation.

Table 40. ASYNCH. WRITE(Address Latch Type) to BURST READ AC CHARACTERISTICS

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tWLR	1	-	clock				

TRANSITION TIMING WAVEFORM BETWEEN READ AND WRITE

Fig.37 ASYNCH. WRITE(Low \overline{ADV} Type) to SYNCH. BURST READ TIMING WAVEFORM
 [Latency=5, Burst Length=4]($\overline{MRS}=V_{IH}$)



(SYNCHRONOUS BURST READ CYCLE)

1. The new burst operation can be issued only after the previous burst operation is finished. For the new burst operation, tBEADV should be met.
2. /WAIT Low(tWL or tAWL) : Data not available(driven by \overline{CS} low going edge or \overline{ADV} low going edge)
 /WAIT High(tWH) : Data available(driven by Latency-1 clock)
 /WAIT High-Z(tWZ) : Data don't care(driven by \overline{CS} high going edge)
3. Multiple clock risings are allowed during low \overline{ADV} period. The burst operation starts from the first clock rising.
4. Burst Cycle Time(tBC) should not be over 2.5 μ s.

(LOW \overline{ADV} TYPE ASYNCHRONOUS WRITE CYCLE - \overline{WE} controlled)

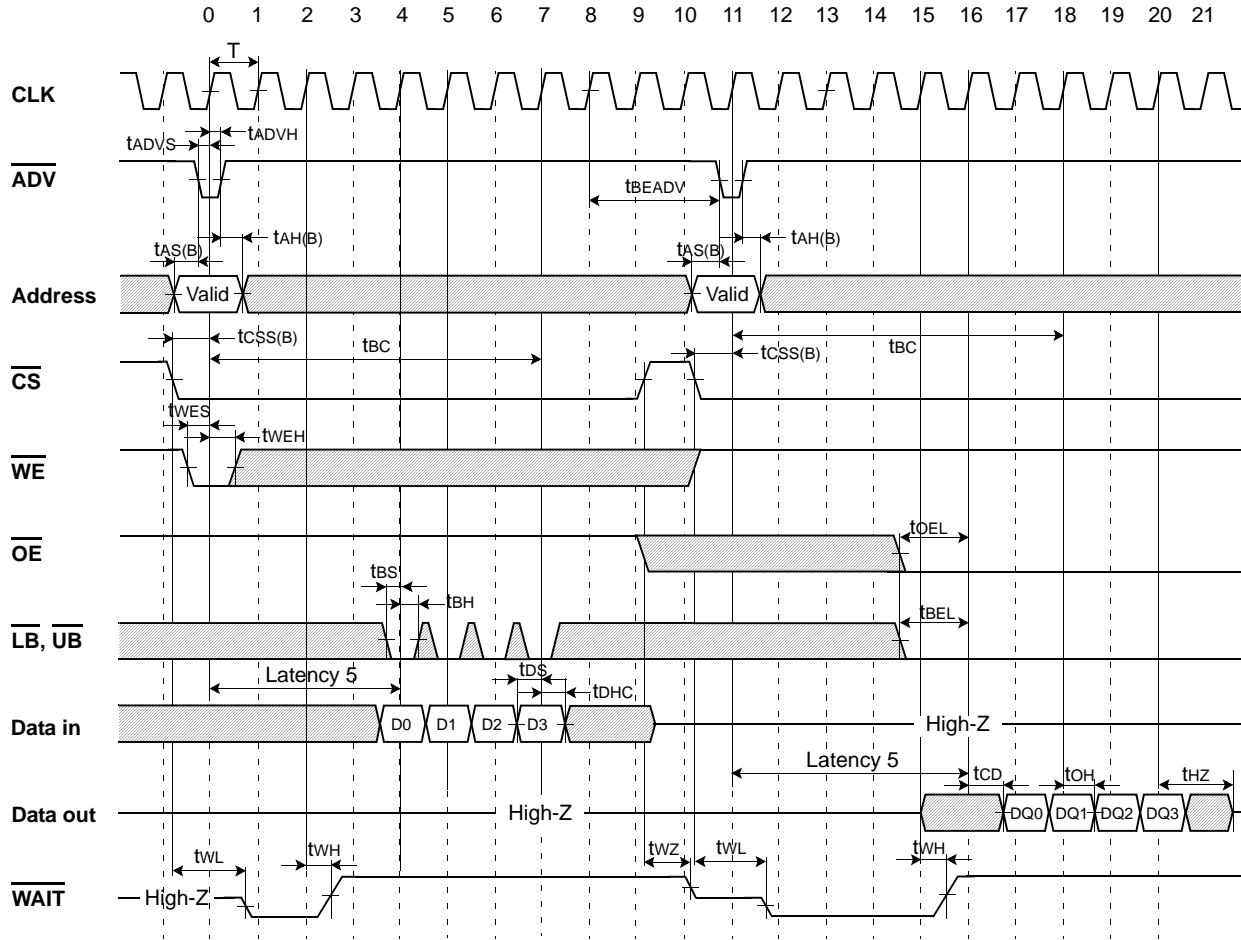
1. Clock input does not have any affect to the write operation if \overline{WE} is driven to low before Read Latency-1 clock. Read Latency-1 clock in write timing is just a reference to \overline{WE} low going for proper write operation.

Table 41. ASYNCH. WRITE(Low \overline{ADV} Type) to BURST READ AC CHARACTERISTICS

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tWLR	1	-	clock	tADHP	5	-	ns

TRANSITION TIMING WAVEFORM BETWEEN READ AND WRITE

Fig.39 SYNCH. BURST WRITE to SYNCH. BURST READ TIMING WAVEFORM
 [Latency=5, Burst Length=4]($\overline{MRS}=V_{IH}$)



(SYNCHRONOUS BURST READ & WRITE CYCLE)

1. The new burst operation can be issued only after the previous burst operation is finished. For the new burst operation, tBEADV should be met.
2. /WAIT Low(tWL or tAWL) : Data not available(driven by \overline{CS} low going edge or \overline{ADV} low going edge)
 /WAIT High(tWH) : Data available(driven by Latency-1 clock)
 /WAIT High-Z(tWZ) : Data don't care(driven by \overline{CS} high going edge)
3. Multiple clock risings are allowed during low \overline{ADV} period. The burst operation starts from the first clock rising.
4. Burst Cycle Time(tBC) should not be over 2.5 μ s.

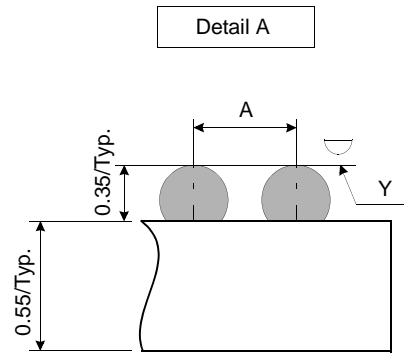
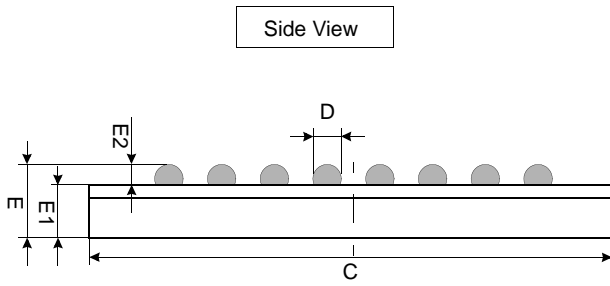
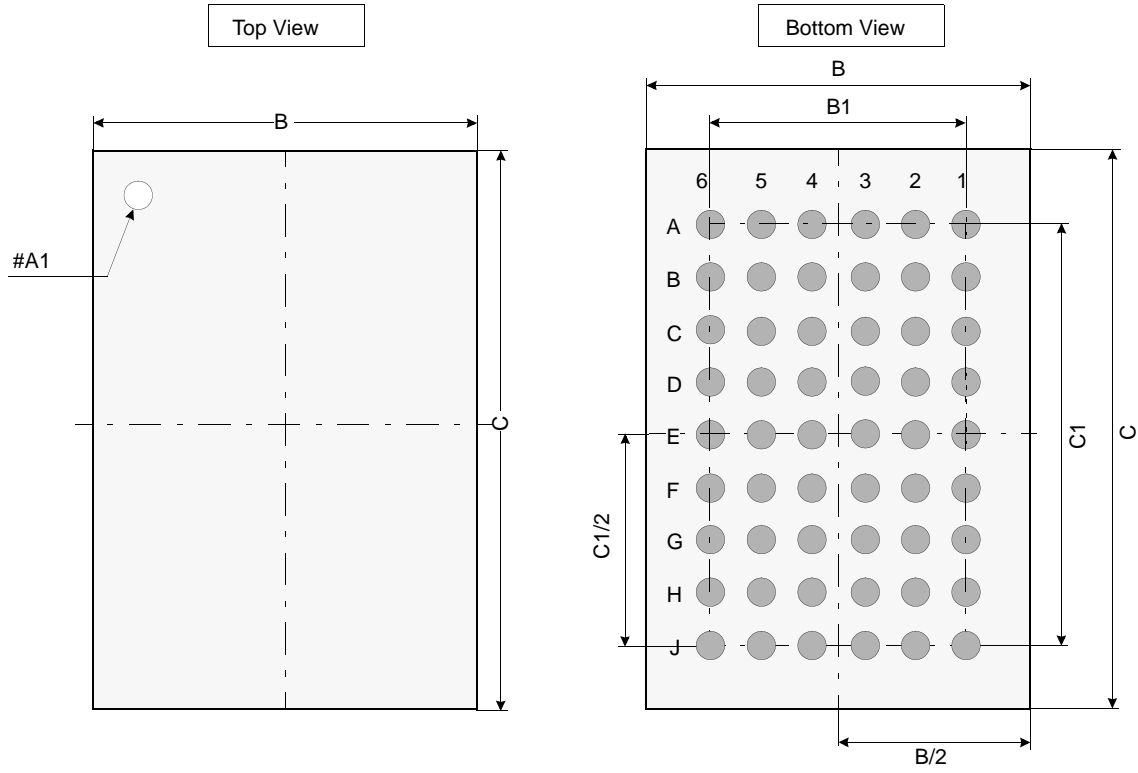
Table 43. BURST WRITE to BURST READ AC CHARACTERISTICS

Symbol	Speed		Units	Symbol	Speed		Units
	Min	Max			Min	Max	
tBEADV	7	-	ns				

PACKAGE DIMENSION

Unit: millimeters

54 BALL FINE PITCH BGA(0.75mm ball pitch)



	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.40	0.45	0.50
E	-	0.90	1.00
E1	-	0.55	-
E2	0.30	0.35	0.40
Y	-	-	0.10

Notes.

1. Bump counts: 54(9 row x 6 column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are ± 0.050 unless specified beside figures.
4. Typ : Typical
5. Y is coplanarity: 0.10(Max)